9 Drift Tube Local Trigger

9.1 Requirements

The muon trigger aims to the identification of the muon and to provide a good measurement of its momentum in order to allow a sharp cut for rate reduction purposes. These tasks are separated in the drift tubes trigger: a local algorithm provides the muon track segments (trigger primitives) inside each station and a regional algorithm links these segments extracting the vector parameters of each identified muon.

The local trigger must immediately resolve time ambiguities and therefore it is required to perform the muon parent bunch crossing identification. Thus each track segment is uniquely assigned to a LHC bunch crossing as soon as it is found. This process must be dead time free in order to avoid any event loss. Besides the trigger dead areas must be negligible, leading to a concept of redundant design.

The existence of punchthrough muons and the need to find dimuons imposes the constraint to be able to find more than one track inside a single station. The two muons have usually different momenta and directions: hence if they are very close inside one station they separate at different stations. A few centimeters wide zone insensitive to dimuons is therefore allowed inside each station.

The momentum cut is more effective as higher resolutions are available at the trigger primitive level. The running algorithms should try to push their resolution as close as possible to the muon chambers resolution.

The trigger requirements are therefore so stringent that the barrel muon detector layout was designed around the trigger.

9.2 System Overview

The block scheme of the first level drift tubes muon trigger primitive generator [9.1][9.2][9.3] inside each muon station is shown in Fig. 9.1.

Each muon chamber is instrumented in the transverse (r,ϕ) plane (hereafter ϕ view) and in the longitudinal (r,θ) plane (hereafter θ view).

The front-end trigger device is called Bunch and Track Identifier (BTI): it performs a rough track reconstruction within each SL and uniquely assigns the parent bunch crossing of the candidate track. The device was realized and prototypes were recently tested.

The BTI is followed by a Track Correlator (TRACO) that is required to associate portions of tracks in the same chamber combining groups of BTIs of the ϕ view among them. The TRACO enhances the angular resolution and produces a quality hierarchy of the triggers.

TRACO trigger data are transmitted to the chamber Trigger Server (TS). Actually the TS is composed by a set of devices (Track Sorter Slave (TSS), Track Sorter Master (TSM) and Trigger Server Theta (TST)) whose purpose is performing track selection in a multitrack environment. The

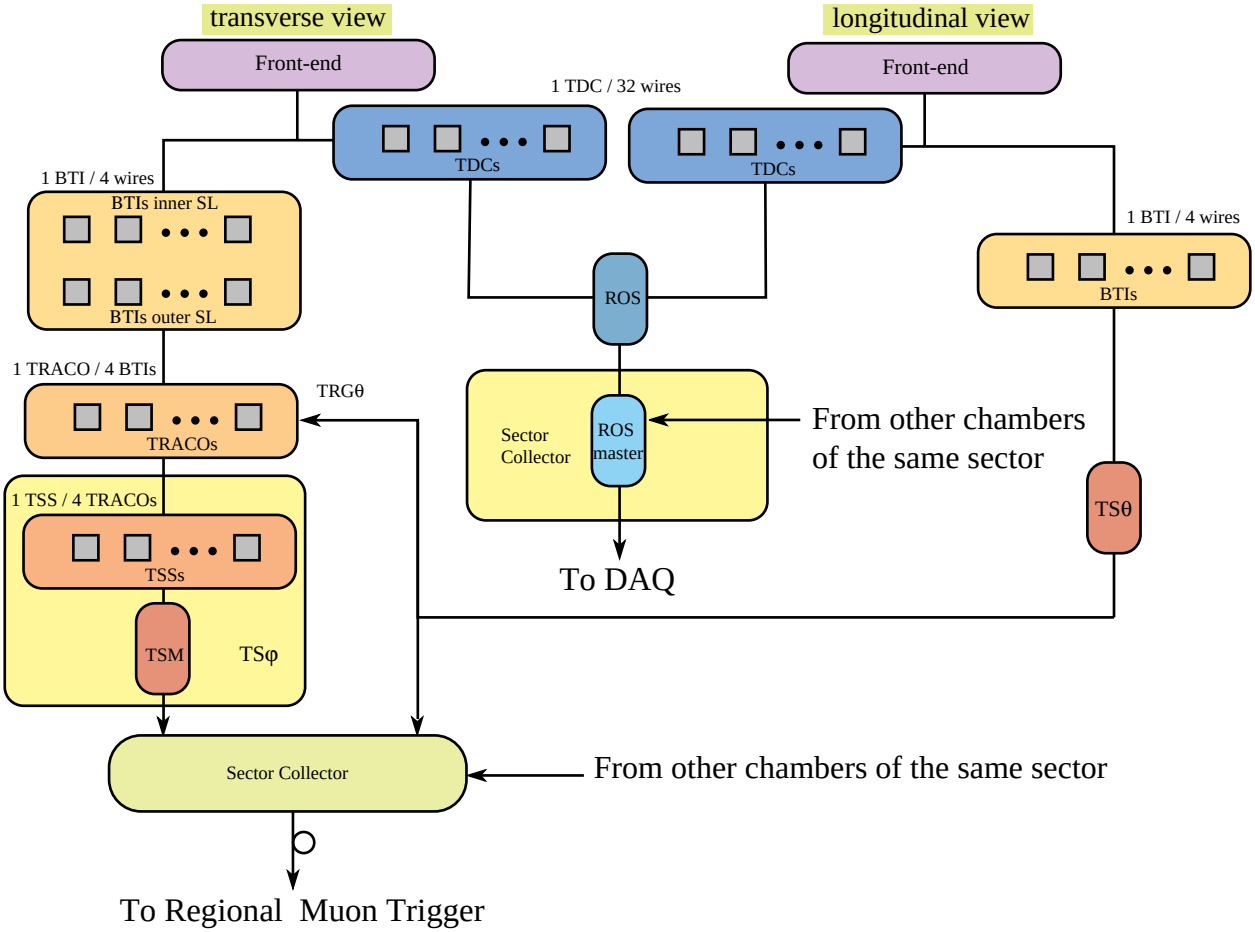


Fig. 9.1: Overview of one barrel muon station electronics layout.

TS of the ϕ view selects two tracks (looking for the lowest bending angle) among all tracks transmitted by the TRACOs; the TS of the θ view sends the wired-or of the BTI trigger outputs to TRACOs for trigger qualification purposes and codes the triggers in a 16 bits string giving all the tracks pointing to the vertex with a position resolution of 16cm and a quality marker.

Data from the four muon stations in each CMS sector are conveyed using LVDS links towards a Sector Collector (SC) that codes the trigger information (track position, bending angle, quality bits) transmitting it to the Regional Muon Trigger using optical links.

9.2.1 Drift Tube Local Trigger Layout

Chamber trigger and readout electronics is lodged in Mini-Crates (MC) mounted on the front side of the chamber, inside the C profile surrounding the honeycomb layer. A pictorial view of the MC without front panels showing its location inside the chamber is given in Fig. 9.2.

Low and high voltage power supplies are lodged on the balconies in crates powering half a wheel each. MCs trigger and readout data in each sector are sent to the Sector Collector (SC) unit that is integrated in the fourth station MC. Chamber trigger and readout electronics is arranged in 128 channel units; only for the first and the fourth stations a 32 channel unit is necessary for a better matching with chamber channel number.

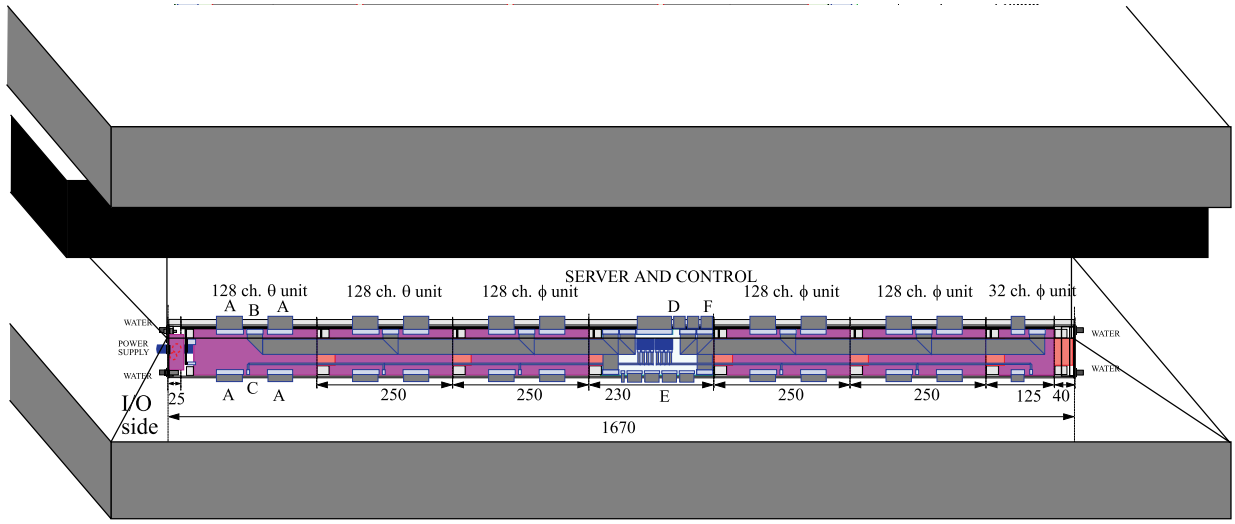


Fig. 9.2: DTbx first station Mini-Crate location.

Inside the MC a Drift Tubes Chamber Control Board (DTCCB) takes care of electronics setup, monitoring and of many control and test functions. One TTC receiver chip is lodged on the DTCCB for clock and broadcast signals distribution. Each DTCCB is connected via a dedicated optical fiber to the Drift Tubes Control Master (DTCM) crate in counting room (see Chapter 9.7). As back-up channel a copper cable connects in parallel all MCs belonging to each half wheel to a Drift Tubes Wheel Control Board (DTWCB) sitting on the balconies. Each DTWCB is connected to the DTCM via dedicated optical fibers. MCs are connected to front-ends of both ϕ and θ SLs and to alignment and RPC electronics for remote controls via two dedicated I2C buses. MCs are cooled by cold water flowing in tubes extruded in the MC aluminum profile along the full length.

9.2.2 Trigger Boards

Trigger electronics is grouped in 128-channel units. An additional 32-channel unit is needed in the first and fourth stations to match the channel number. There are three types of different boards: two for the ϕ view, a 128-channel unit called PHITRB128 and a 32-channel one called PHITRB32. PHITRB128 contains 32 BTIs assembled in 8 multi-chip modules (BTIM) connected to 4 TRACOs and one TSS (Fig. 9.3), while PHITRB32 contains 2 BTIMs, one TRACO and one TSS (Fig. 9.4).

Only a 128-channel unit called THETATRB containing 32 BTIs assembled on 8 BTIMs exists for the θ view (Fig. 9.5).

Front-end signals are received through the faced Readout Board, where LVDS to CMOS translators are located, while trigger data are sent to the TS via a fine-pitch 40 lines flat cable. Fine pitch lateral connectors are used for neighboring unit communications of detector signals and of chamber control signals coming from the central Server and Control Unit (SCU).

Trigger Board power supply is internally stabilized to 3.3V by a low drop regulator. The internal regulator has power supply protection circuitry with over and under voltage tolerance up to +-40V and overcurrent limit with a “retriggerable fuse” function useful for latch-up protection.

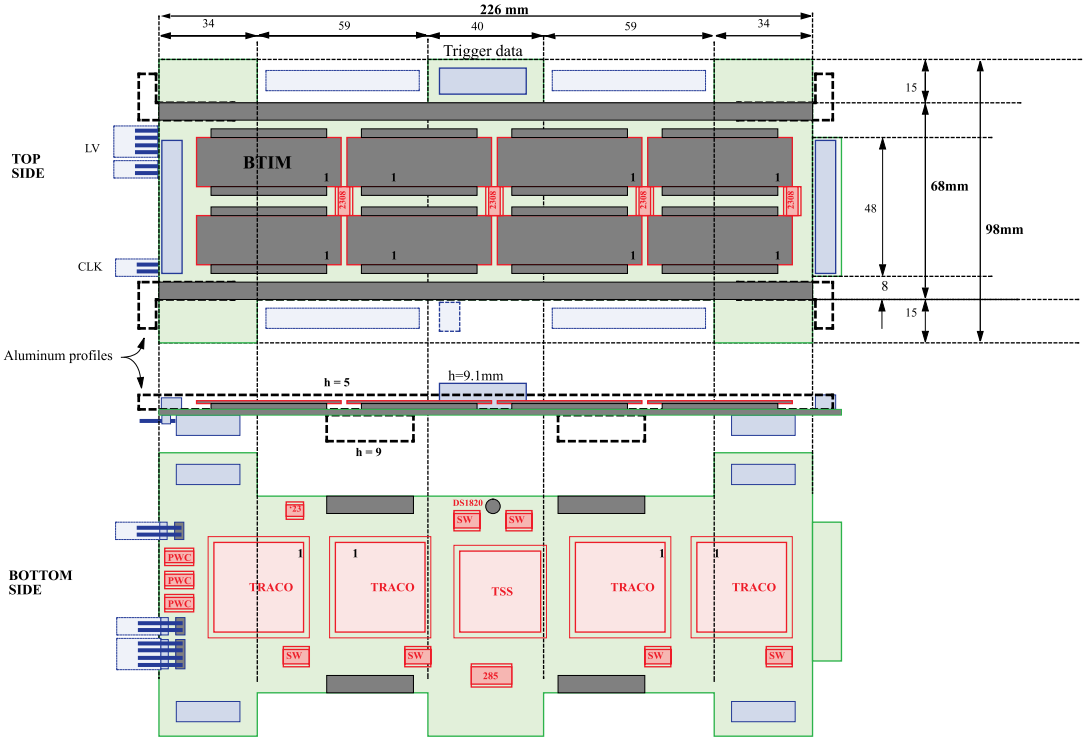


Fig. 9.3: Layout of PHITRB128, the 128 channels board for DTbx transverse plane trigger

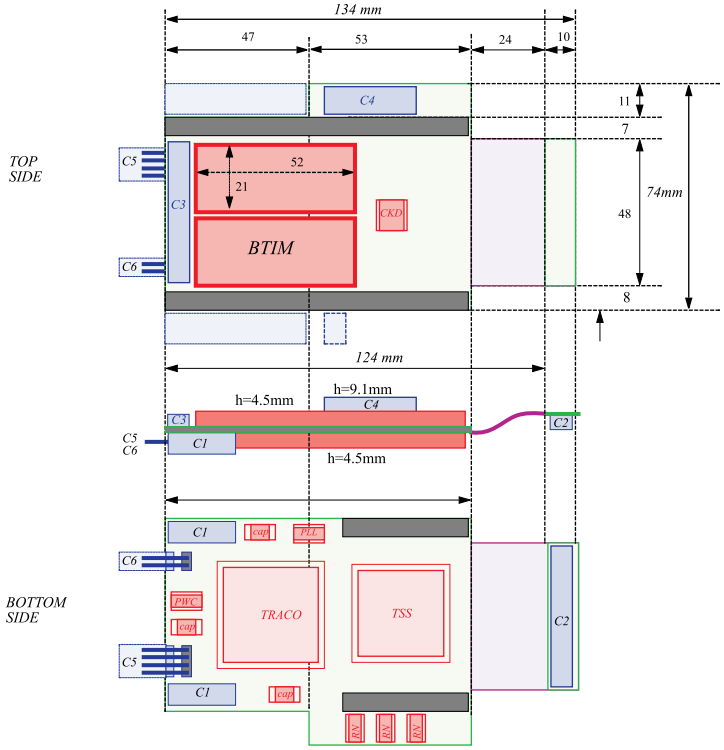


Fig. 9.4: Sketch of PHITRB32 layout, the 32 channels board for DTbx transverse plane trigger

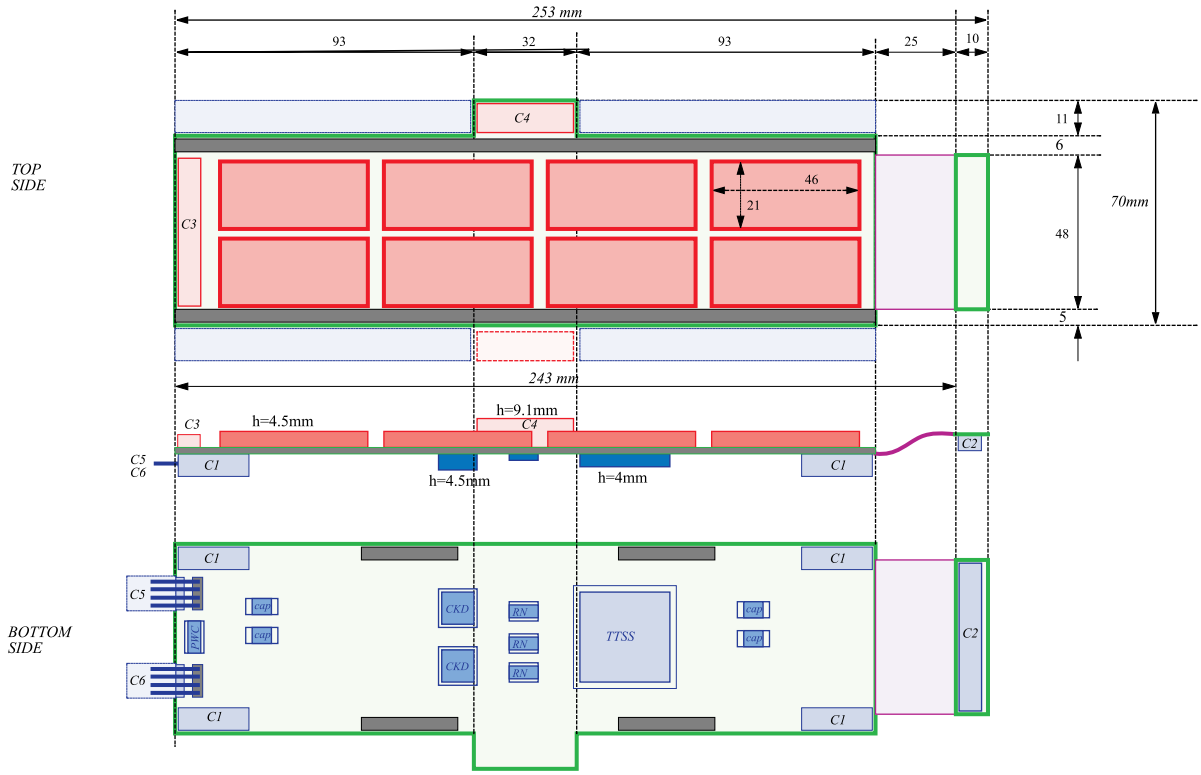


Fig. 9.5: Layout of THETATRB, the 128 channels board for DTbx longitudinal plane trigger

Each Trigger Board can be shut off independently thanks to an “intelligent” on board regulator and input signal isolation logic. Local power supply measurement and control is accomplished by the Control Board that takes care of device turn-on and turn-off sequences.

Clock is distributed using Pseudo-ECL signals on twisted pair cables. One clock input with low skew is foreseen per Trigger Board. A low-skew clock distribution tree, consisting of PLLs and multiple drivers, is implemented in each Trigger Board. The maximum allowed skew from TTC output to ASIC input is about 1ns.

Trigger Boards can be tested at many levels using a JTAG bus and on-board self-test features. The Control Board can address a single Trigger Board for JTAG access, up to a maximum of 16 units, in order to reduce the component chain. A production assembly test is foreseen using boundary scan and on-board functional tests using event emulation capabilities integrated in BTI test logic. Once the Trigger board is programmed in Test Mode, emulation data, consisting of the delays in 12.5 ns steps of event hits, are downloaded to all BTIs via JTAG. A trigger command issued via JTAG and internally synchronized with the 40 MHz clock starts the test sequence. Trigger data can be latched at Trigger Board output or readout via JTAG, downloading the content of snap registers integrated in all ASICs. This kind of functional test can be repeated for assembled MCs allowing a full test of trigger functionality without any external test pattern generator.

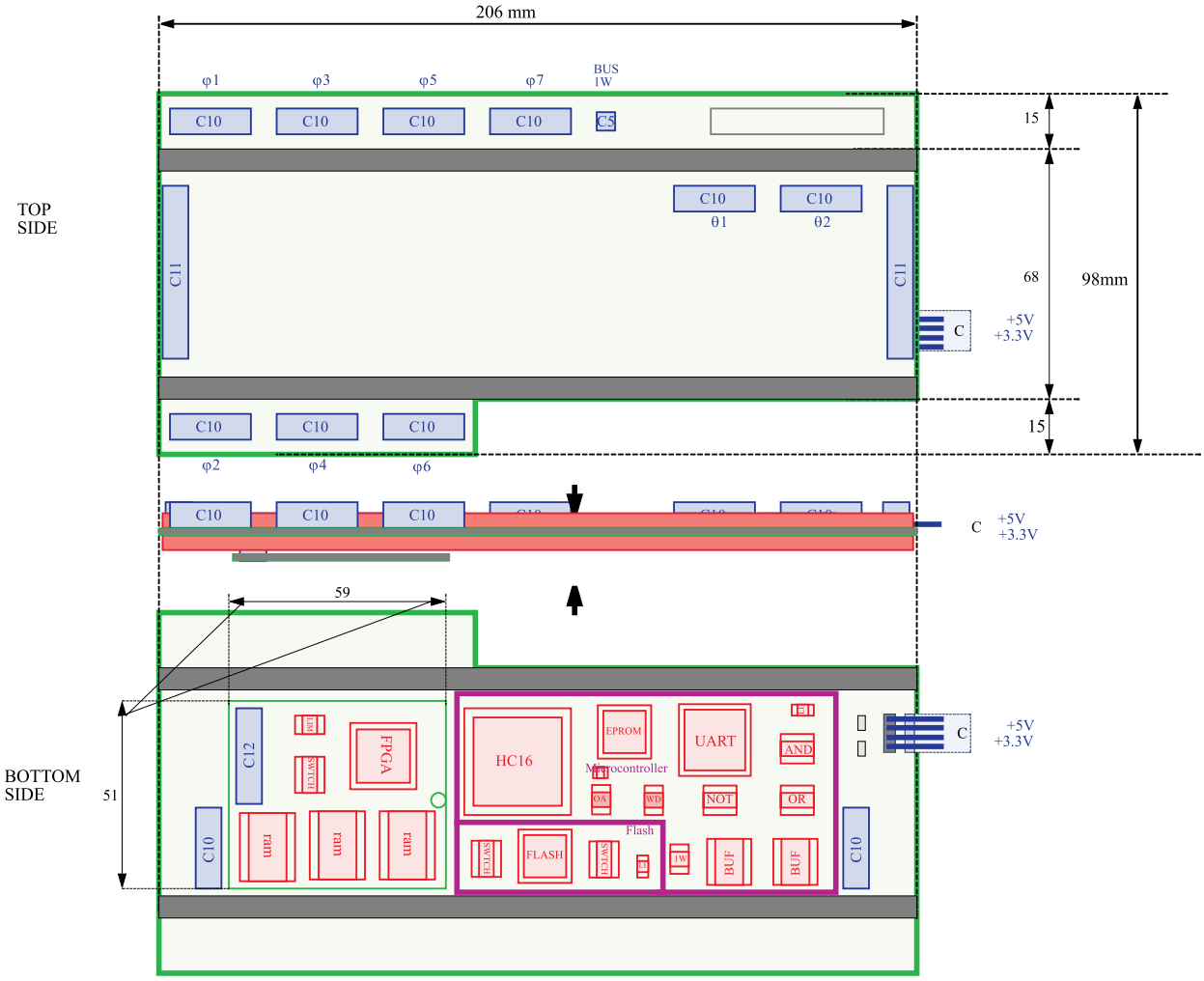


Fig. 9.6: Sketch of the layout of the Server Board in the SCU of DTbx mini-crate electronics.

9.2.3 Server Board

There is one Server Board per MC: the Track Sorter Master consisting of three chips is lodged on it. The Server Board is part of the Server and Control Unit.

This unit is powered with three separated 3.3V lines, one per ASIC, in order to maintain the highest possible redundancy. Overcurrents, on power supply lines, are protected by precise current monitors with fast shut off capability.

Server Board clock phase is adjustable with respect to the Trigger Board clocks to take care of signals synchronization. The Server Board layout is shown in Fig. 9.6.

9.3 Bunch And Track Identifier (BTI)

The BTI is directly interfaced to the front-end of the muon chamber system. It generates a trigger at the alignment of the hits produced in the group of drift tubes interested by the muon. The coincidence of these hits happens at fixed time after the muon traversed the array of drift tubes allowing bunch crossing identification. The BTI can extract the full track information (position and direction).

9.3.1 Working Principle

The Bunch and Track Identifier is the implementation of a trigger device based on the generalized mean-timer method [9.4]. It was explicitly developed to extend the technique to work on groups of four layers of staggered drift tubes, aiming to the identification of the tracks giving signals in at least three out of the four measurement planes.

This method relies on the fact that the particle path is a straight line and the wire positions along the path (the measurement points) are equidistant. Therefore, considering the drift times of any three adjacent planes of staggered tubes (e.g. cells in layers A, B and C of Fig. 9.7), the relation

$$T_{MAX} = \frac{T_A + 2T_B + T_C}{2}$$

where T_{MAX} is the maximum drift time to the wire, holds independently of the track impact point and angle of incidence. Actually the BTI digitizes the time T_s after particle detection at 80 MHz frequency and at every clock count computes the apparent drift time $T = T_{MAX} - T_s$, where T_{MAX} is a programmable parameter depending on drift velocity. This calculation gives the real drift times only at the time T_{MAX} after particle crossing. Therefore the digitized times have

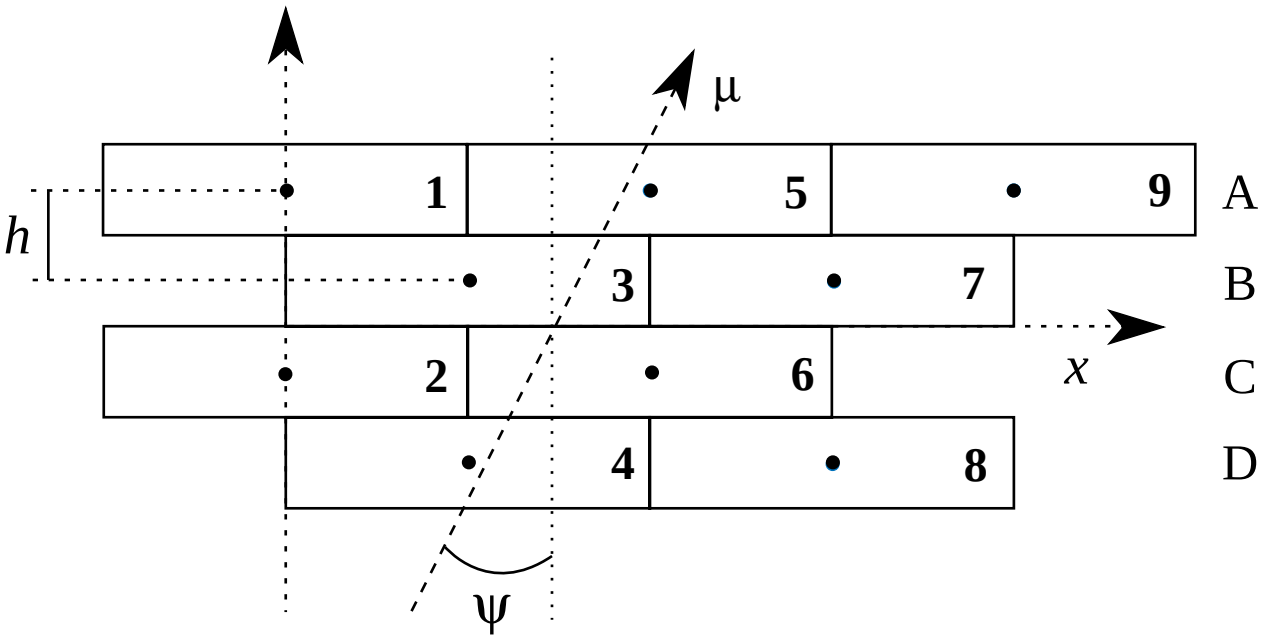


Fig. 9.7: BTI geometric layout showing the channels allocation and important parameters.

values satisfying the relation only at that clock count, while the relation does not hold true at any other time.

This constant time difference, between the particle crossing and the detection of the relation validity, allows the identification of the parent bunch crossing.

In fact it occurs that at the time T_{MAX} after muon crossing the drift times are aligned: i.e. the hits form an image of the muon track, thus allowing the extraction of the full track information (track impact position and direction).

Extending the method to four layers, implies that the bunch crossing identification is possible even if the drift time of a tube is missing, due to inefficiency, or wrong, due to the emission of a δ-ray masking the good hit, since there are still three useful cells giving the minimum requested information. The mean timer method is also insensitive to all uncorrelated single hits and it is therefore well-suited to a high radiation environment.

9.3.2 Algorithm Description

Each BTI is connected to nine wires allocated as shown in Fig. 9.7. Each SL is equipped with one BTI every four wires and therefore the BTIs are overlapped by five wires, i.e. the next BTI will start from cell labeled 5 in Fig. 9.7. This overlap assures the redundancy needed to limit the inefficiency in case of a BTI failure.

The evaluated parameters are the position, computed in the SL centre, and the angular k-parameter $k = h \tan \psi$, with ψ being the angle of the track with respect to the normal to the chamber plane in the transverse projection and $h = 13mm$ being the distance between the wire planes.

The actual BTI candidate track finding algorithm computes in parallel several track patterns hypotheses: a pattern is identified by a sequence of wire numbers and labels stating if the track crosses the tube on the right or on the left of the given wire (e.g. in Fig. 9.7 the track corresponds to the pattern 5L3R6L4R). Any given pattern includes six couples of planes (AB, BC, CD, AC, BD, AD), each one providing a measurement of the position (through a *x-equation*) and of the k-parameter (through a *k-equation*) of the track.

The equations are computed at every cycle using the hit arrival time with 12.5ns resolution. At any clock cycle the value of a *k-equation* corresponds to a rough measurement of the track direction at that cycle and is time dependent. Therefore each couple included in a pattern gives its own measurement of the track direction at every clock cycle: the hits are aligned when, after applying a couple dependent proportional factor, the values of the k-parameter computed for each couple are equal.

Hence at every clock cycle the whole set of *k-equations* is computed and a BTI trigger is generated if at least three of the six k-parameters associated to any of the patterns are in coincidence. The coincidence of the *k-equations* values is verified within a programmable tolerance window. This tolerance is defined according to the resolution of each couple that in turn depends on the distance between the wires and was chosen to allow a maximum cell linearity error equivalent to 25ns. The coincidence allows the bunch crossing identification owing to the time-dependence of the *k-equations* value.

If there is a coincidence of all the six k-parameters, the trigger corresponds to the alignment of four hits and it is marked as High Quality Trigger (HTRG), while in any other case,

with a minimum of three coincident k-parameters, it is due to the alignment of only three hits and it is marked Low Quality Trigger (LTRG). The angular resolution is track pattern dependent and is generally worse for LTRGs.

If several track patterns give a response, the HTRG is chosen as the triggering track pattern. If there is more than one HTRG or the triggers are all LTRGs, the first one, in an arbitrarily defined order, is selected.

The request of the alignment of any three hits is a substantial source of background, since it introduces effects creating false triggers. There is a probability that the alignment of four hits at some clock step produces the alignment of only three of them at the step just before or after the HTRG signal, thus generating *ghost* LTRG candidate tracks. There is also some probability that a random LTRG could happen at any clock step with some fancy k-parameter due to the left-right ambiguity, that is duplicating the possible choices for every hit. Finally the δ-rays produced inside the cell will provide wrong time measurement enhancing the probability of an out of time trigger generated using the wrong measurement.

The noise reduction of the former kind of *ghosts* is obtained issuing the LTRG signal only if at the neighbouring steps there is not any HTRG generated: this mechanism is called Low Trigger Suppression (LTS). The noise reduction of the latter kind of *ghosts* is obtained acting on tolerances in the association phase of the following stages of the trigger. These algorithms do not add any latency to the BTI flow.

The impact position of the muon is not entering the track selection algorithm and it is computed only at the end of the process and only for the selected triggering pattern.

Position and angular resolution depend on the drift velocity and on the sampling frequency of the device. The drift velocity without magnetic field and for the gas mixture foreseen in the drift chambers (Ar/CO_2-85/15) is 56μm/ns and the sampling frequency is 80MHz. Under these conditions the angle is measured with a least count better than 60mrad and the position is measured with a least count of 1.4mm.

With the present geometric parameters of the chamber the BTI equations are fully covering the angular range up to $\psi_{MAX} = \pm 45^{\circ}$.

9.3.3 Hardware Implementation

The Bunch and Track Identifier was implemented in an ASIC, the best compromise between cost and performance. A block scheme of the BTI chip is shown in Fig. 9.8.

The *Input Shapers* block is the interface to the 9 discriminated wire signals coming from the analog front-ends. An input latch is triggered by the rising edge of the signal, accepting a minimum pulse width of 3ns. Outputs are stretched to a programmable duration; during this time the input shaper is not retriggerable in order to reject high frequency double pulses. This parameter is close to T_{MAX} and must be set according to drift velocity to minimize tube dead time.

In the *Pattern Logic* blocks all track patterns are evaluated in parallel. For each wire couple the Equations Counters compute the k-parameter and the position of the crossing track according to the reference system introduced in Fig. 9.7.

In the *Pattern Comparator* block the parent bunch crossing is identified looking for a matching of the k-parameters computed by the six equation counters relative to the four crossed

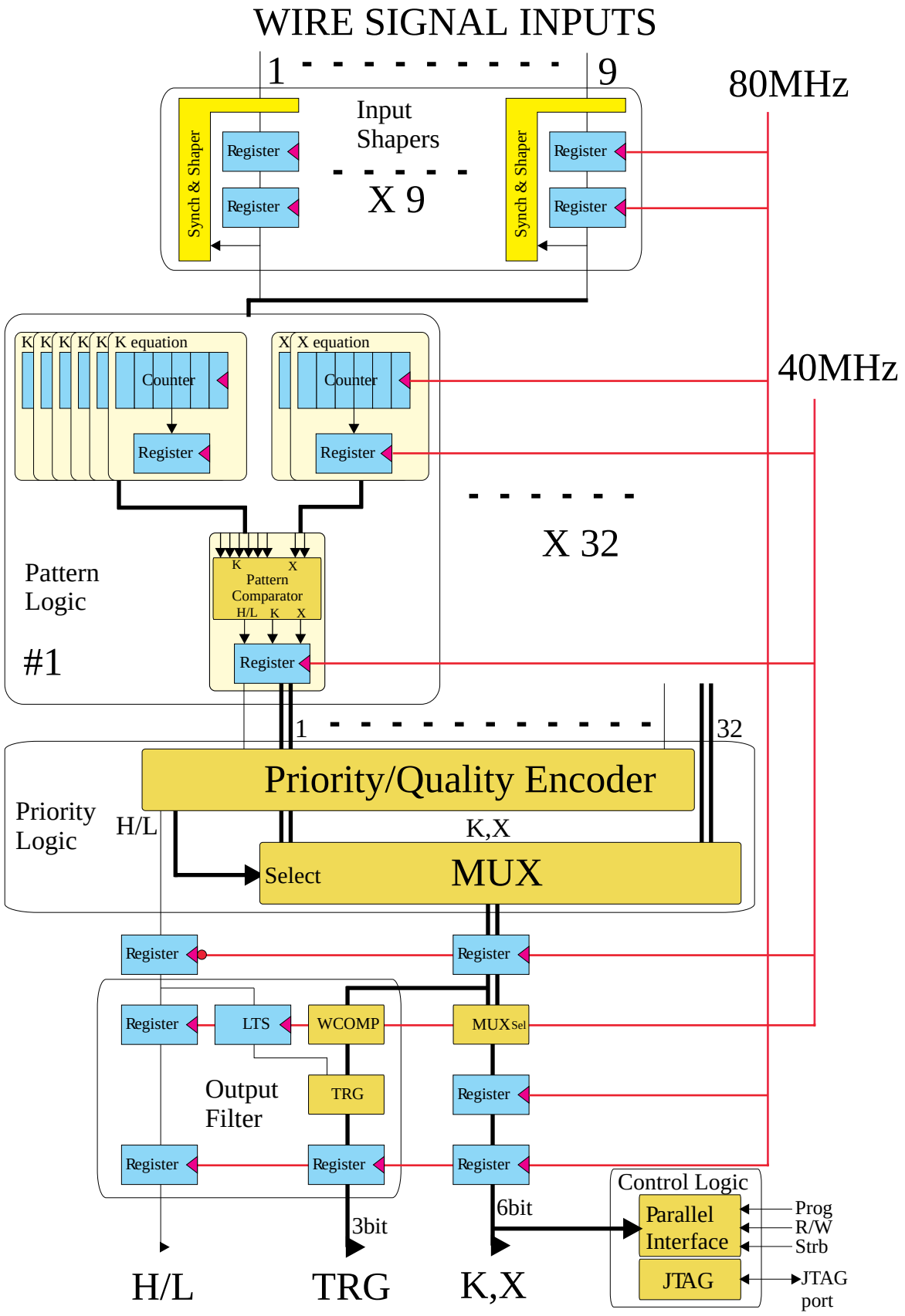


Fig. 9.8: BTI block scheme.

tubes. The output is the matching value K, the position X and the quality bit H/L. The use of a quality bit allows the next device in the trigger chain to distinguish between clean tracks (alignment of four hits, i.e. six coincident k-parameters) and potentially wrong triggers (three out of four aligned hits, i.e. at least three coincident k-parameters) where can be classified most of the *ghost triggers*.

If several track patterns give a trigger at the same time, only one is selected by the *Priority Logic*, preferring a high quality track and using a default encoded order in case of multiple triggers with the same quality.

The BTIs send their data to TRACOs that associate the track segments and performs noise rejection. Indeed each BTI of the chamber outer SL is interfaced to three TRACOs. In order to reduce the probability to generate multiple triggers from a single track transmitting three copies of it, an angular filter was included and programmed to send to each TRACO only those tracks that could be fully contained in it. The trigger strobe is split into three signals activated only if the track k-parameter is within the relative programmable window of each TRACO. The quality bit line and the k-parameter/position bus are common to the three TRACOs. The BTI trigger output bus consists of the three trigger strobes, the quality bit and the 6 bit data bus where k-parameter and position are multiplexed at the clock speed.

In order to reduce the number of *ghost triggers*, the cancellation of LTRGs in the range (-1bunch crossing,+8bunch crossings) around a high quality trigger (Low Trigger Suppression) is a very efficient solution. The LTS logic block is latency inexpensive because it was inserted in the *Output Filter* pipeline, in parallel with the window comparator logic.

The *Control Logic* block contains a JTAG interface and a bidirectional parallel interface.

Details on the integrated circuit design and characteristics are reported in [9.5].

9.4 Track Correlator (TRACO)

The BTI is followed in the electronics chain by a Track Correlator (TRACO) [9.6] that is required to associate portions of tracks in the same chamber relating predefined groups of BTIs among them. The TRACO interconnects the two SLs of the φ view. It receives the information from the BTI devices connected to it and tries to find the couple of BTI track segments that fits the best track, linking the inner layer candidates to the outer layer ones.

The introduction of this device is necessary since the BTI is intrinsically a noisy device and therefore a local preselection and a quality certification of the BTI triggers is required. Furthermore the number of BTIs per chamber is around few hundreds and it is not possible to connect together all the channels to perform any preselection at chamber level.

9.4.1 Algorithm Description

The number of BTIs connected to a TRACO is limited from the size of the chip and it is determined by the acceptance requirement. The current design connects four BTIs of the inner SL to twelve BTIs of the outer SL allocated as shown in Fig. 9.9, assuring a full coverage until ψ_{MAX}.

The algorithm starts selecting, among all the candidates in the inner SL and the outer SL independently, the best track segment, according to preferences given to the trigger quality (H/L) and to the track proximity to the radial direction to the vertex (i.e. its p_T).

Then it computes the k-parameter and the position of a correlated track candidate. The compatibility between the k-parameters of the selected track segments in the inner and outer SLs and the correlated track is checked against a programmable tolerance.

The internal parameters computed for the correlated tracks are:

$$\begin{cases} k_{COR} = \dfrac{D}{2}\tan\psi = x_{inner} - x_{outer} \\ x_{COR} = \dfrac{\left(x_{inner} + x_{outer}\right)}{2} \end{cases}$$

Owing to the long lever arm between the two SL the angular resolution of a correlated track candidate is 10mrad for the nominal drift velocity, thus significantly improving the BTI precision, while the resolution on the position remains unchanged.

These parameters are converted, using programmable look-up tables, to the chamber reference system: position is transformed to radial angle ϕ and k-parameter to bending angle ϕ_b as defined in Fig. 9.10.The chosen track is forwarded to the chamber TS, for further selection.

If the correlation fails the correlator forwards an uncorrelated track following a preference list that includes the parent SL (IN/OUT) and the quality bit (H/L) of the two tracks selected for correlations.

If no correlation is possible since there is no candidate in one SL, the uncorrelated track is anyway forwarded.

The track is output on a bus, using 10 bits for the bending angle and 12 bits for the radial angle and it is accompanied by three quality bits identifying HH, HL, LL, H_i, H_o, L_i, L_o track candidates with obvious symbols meaning.

A further preference selection can be activated to connect the trigger generated in the φ view to the triggers generated from the BTIs in the θ view. In particular, since the noise generated from the BTI algorithm is of LTRG quality, a programmable coincidence between the two views is foreseen to certify the uncorrelated LTRGs.

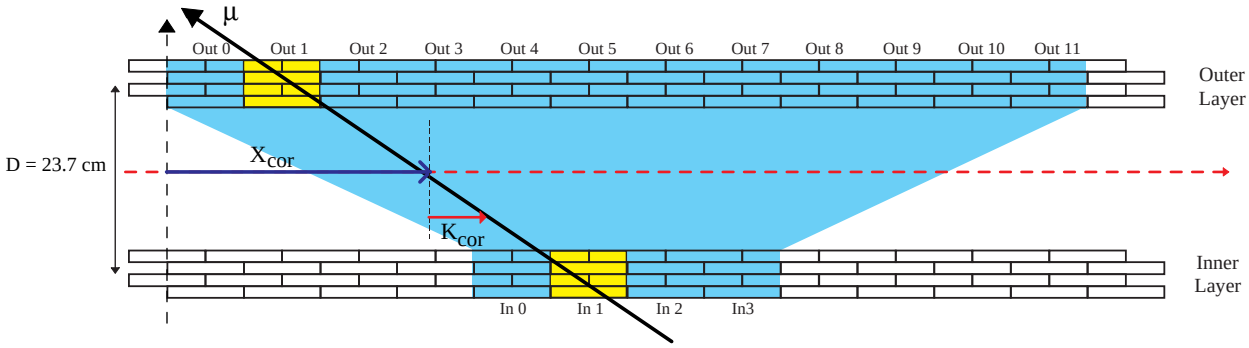


Fig. 9.9: Track Correlator layout.

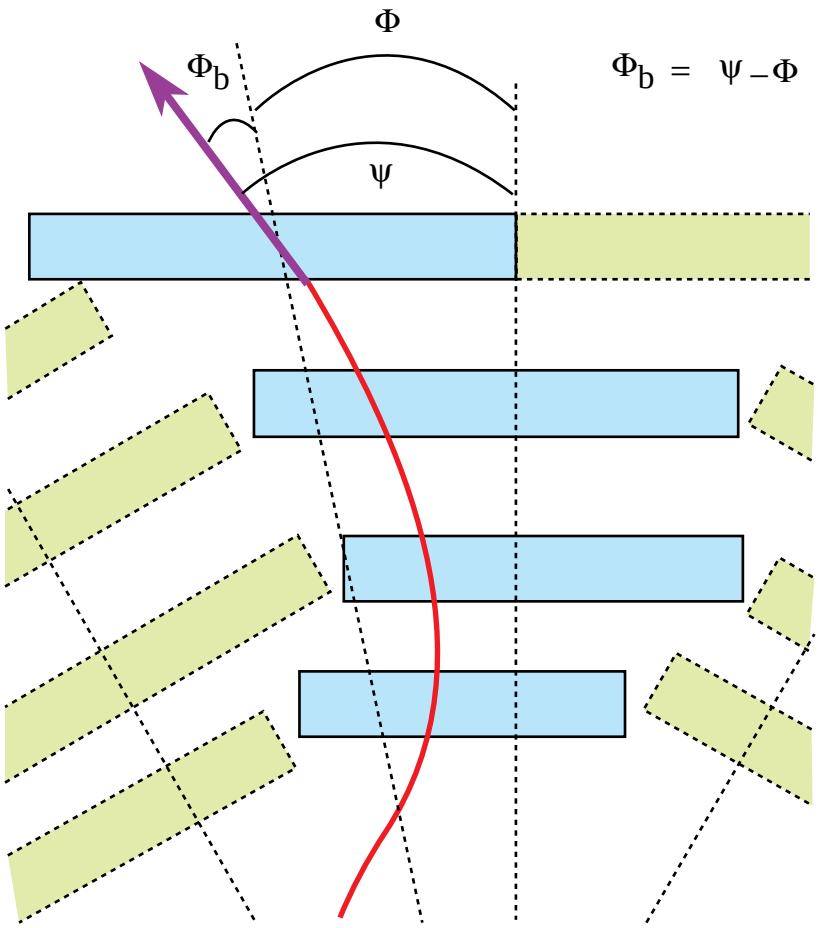


Fig. 9.10: Definition of TRACO output parameters.

In order to allow the identification of two muons inside the same correlator, the same algorithm is applied twice to the data received from the BTI. Therefore sometimes a second track is forwarded to the chamber TS. The programmability of the preferences for the choice of the First Track and the Second Track are completely independent, although we believe that the same criteria should apply.

A further selection is needed in the case that more than one TRACO inside a chamber give a trigger. The communication between the TRACOs and the chamber TS to allow this decision is done using a Preview information, in order to minimize the time needed for calculations of the whole trigger chain. A copy (called Preview) of one of the candidates chosen for correlation is sent to the TS according to the programmed H/L and IN/OUT selection flags, before starting any correlation calculation. The TS selection is based on the quality of the Preview (given by the BTI resolution) of the various candidates.

9.4.2 Hardware Implementation

The block diagram of the TRACO operations is given in Fig. 9.11. In the following paragraphs we shall describe the TRACO algorithm referring to the flow of this diagram.

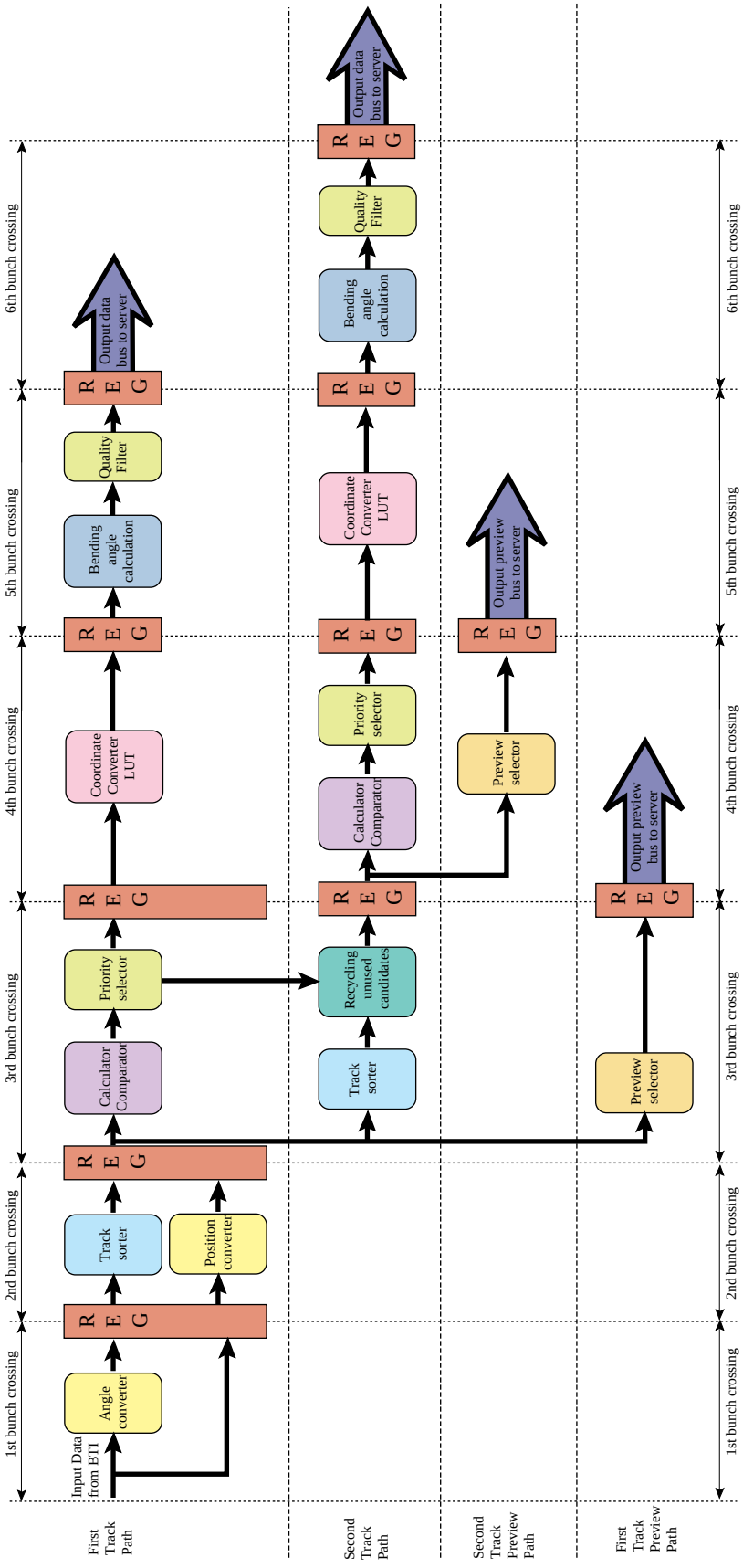


Fig. 9.11: TRACO block scheme

There are four *data flows* inside the TRACO: two track calculation flows and two track Preview flows.

In order to allow the identification of two muons inside the same correlator, the TRACO algorithm is applied twice to the data received from the BTI. Therefore inside the TRACO there are two parallel flows delayed by one cycle: the first path computes a First Track, choosing between all the BTI candidates, while the delayed path computes a Second Track from all unused candidates. The programmability of the preferences, described in details later, for the choice of the First Track and the Second Track are completely independent, although in principle we believe that the same criteria should apply.

A further selection is needed in the case that more than one TRACO inside a chamber give a trigger. The communication between the TRACOs and the chamber TS to allow this decision is done using a dedicated Preview data bus for each track, in order to minimize the time needed for calculations of the whole trigger chain. A copy of the k-parameter of one of the candidates chosen for correlation is sent to the TS according to the programmed H/L and IN/OUT selection flags. The TS selection is based on the quality of the Preview of the various candidates. The Preview data are coded in 9 bits: five bits for the module of the k-parameter, one bit for the track quality (H/L); one bit identifying First/Second track; one bit identifying Inner/Outer layer; one bit identifying Correlated/Uncorrelated track candidate.

The *Input Register* (16 x 8bits) receives and latches the data values and the qualification flags from the BTI chip. The TRACO collects the inputs from 16 BTIs (four from the inner layer and twelve from the outer layer).

The input data bus from each BTI contains the k-parameter and the position in the BTI coordinate system, multiplexed at 80MHz on the same lines (6 bits wide). Two extra flags are provided: the trigger quality (H/L) and the strobe.

The *Angle and Position Converter* module receives the k-parameter 6 bits input word from the BTI and converts it into local radial coordinates ($k_{local} = k_{BTI}$ - RAD - offset). The RAD parameter is a 6 bits load value, depending on the geographical position of the correlator, i.e. the k-parameter of its center. The offset is a programmed value dependent on drift velocity needed by the BTI for its calculations. The converted angle is used for internal calculations and sent on the Preview bus to the TS for further track selection.

Each BTI position is converted to TRACO position, offsetting by the appropriate geographical value. An additional SL shift parameter is provided to correct for eventual construction misalignments of the two SLs.

The *Sorter* module receives the converted angle and selects the candidate with the smallest angle,i.e. the angle closest to the local radial direction. There is one sorter for the four inner BTIs and another for the twelve outer BTIs, hence the choice is done twice independently on the two φ SLs. The sorting operation can be programmed to select the biggest angle instead of the smallest one, and/or to give preference to candidates tagged with the HTRG quality flag.

Two other sorters for the Second Track path exist.

The *Calculator and Comparator* module computes the k-parameter and the position of the correlated candidate. It transforms the inner and outer k-parameter of the two independently selected track segments into the correlator coordinates system and computes the correlated track

parameters.The angular resolution of a correlated track candidate is 10mrad for the nominal drift velocity, thus improving the BTI value, while the resolution on the position is unchanged.

A second step compares the three candidates (single inner, single outer, correlated) to set the correlated flag. If the correlated track fits inside the programmed acceptance window this flag is raised.

The *Priority Selector and Preview Selector* module selects one of the candidates according with some programmed information.

If the correlation was successful the priority selector chooses the correlated candidate and forwards its parameters to the further stages. If the correlation fails the correlator creates an uncorrelated track following a preference list that includes the parent superlayer (IN/OUT) and the quality bit (H/L) of the two candidate tracks. If no correlation is possible since there is no candidate in one Superlayer, the existing uncorrelated track is still accepted.

The trigger quality H/L and the IN/OUT preference selections are chosen according to the following programming masks: high level trigger mask (HTMSK), low level trigger mask (LTMSK), Superlayer mask (SLMSK).

The First Track priority selector or the Second Track priority selector treats the best inner candidate, the best outer candidate and the correlated candidate considering the trigger quality and all the masks. An equivalent priority selector is implemented for the Preview path. The Preview priority selector treats the best inner and best outer candidates, but only considers LTMSK and SLMSK.

A further preference selection can be activated to connect the trigger generated in the ϕ view to the triggers generated from the BTIs in the θ view. Activating this preference a programmable coincidence between the two views is foreseen to certify the uncorrelated triggers. In particular, since the noise generated from the BTI algorithm is concentrated in the LTRGs, this coincidence is requested by default for the LTRGs and it is optional for the HTRGs.

The priority selector sends only one candidate towards the output bus, and generates a three bits qualification code as shown in Table 9.1.

Two candidates are needed to fit a correlated track, one from the inner superlayer and another from the outer one. If the correlated track does not satisfy the acceptance value, one of the track candidates selected to try the correlation is forwarded as the First Track choice and the other can be reused for the Second Track calculations. This task is performed in the *Recycling unused candidates* module. This feature can be software disabled.

The two selected tracks are output on the same bus at consecutive bunch crossings. Therefore it is possible that a Second Track from the bunch crossing *n* is computed at the same time of a First Track from the bunch crossing *n+1*. A First Track choice has always priority on the output bus and therefore overlaps the Second Track from bunch crossing *n*. The *Mixer* block performs this choice and activates a flag if an overlap occurs.

Inside the *Coordinate converter and bending angle calculation* block the internally calculated position and k-parameter are converted, to the chamber reference system: position is transformed to radial angle ϕ and k-parameter to bending angle ϕ_b as defined in Fig. 9.10.

This task is performed with direct access to two programmable look-up tables. The first look-up table is used for conversion of the local correlator position coded in 9 bits to the track radial

Table 9.1: Codes for output track quality identifier.

Description	Symbol	Code
HTRG on inner and outer layer	HH	6
HTRG on inner or outer layer and LTRG on inner or outer layer	HL	5
LTRG on inner and outer layer	LL	4
HTRG on outer layer	H_o	3
HTRG on inner layer	H_i	2
LTRG on outer layer	L_o	1
LTRG on inner layer	L_i	0
Null track		7

angle ϕ coded in 12 bits. The second performs the conversion from the k-parameter coded in 10 bits to the angle ψ coded in 10 bits.

A further block performs the computation of the bending angle $\phi_b = \phi - \psi$.

Some filtering functions are performed in the *Quality Filter* block to select the output value driven to the chamber server. These functions include an uncorrelated Low Trigger Suppression and a programmable tolerance window for the bending angle output value. The filters will be discussed in detail in Chapter 9.11.2.

The selected track is output on a bus, using 10 bits for the bending angle and 12 bits for the radial angle and it is accompanied by three quality bits identifying HH, HL, LL, H_i, H_o, L_i, L_o track candidates.

Data output bus provides one track at each clock cycle, with up to two tracks per bunch crossing at consecutive clock cycles.

The latency for the First Track is five cycles, while Second Tracks are output after six cycles.

9.5 Trigger Server (TS)

The TS [9.7] has to select the two best trigger candidates among the track segments selected by all TRACOs in a muon station and send them to the Sector Collector, where they will be forwarded to the Regional Muon Trigger.

The TS has to fulfill the following requirements:

– since much of interesting physics has two close muons that can hit the same muon station, much emphasis should be put on the efficiency and purity of both selected segments. The

selection should be based on both the bending angle and the quality of the track segment and selection priorities should be configurable.

- it has to reject fakes eventually generated by TRACOs using a configurable fake rejection algorithm.
- the processing time must be independent on the number of TRACOs in the station.
- the TS should be able to treat pile-up events.
- since only one TS is mounted on each station, redundancy should be put into it, since it represents the bottleneck of the on-chamber trigger devices.

The TS is composed by two subsystems: one for the transverse view (TSϕ) and the other for the longitudinal view (TSθ). The TSθ has to detect triggers produced by the 64 BTIs which equip the SL in the θ view. This information is sent to the TRACOs of the ϕ view and can be used there as a validation of a trigger in order to reduce background. Besides, a pattern of the track segments found in the longitudinal view has to be sent to the Regional Trigger [9.8]. The TSθ consists of groups of OR of BTI hits.

The TSϕ is the real processing system.

The number of TRACOs in a station can be quite large: as much as 25, for the largest station. Each TRACO transmits to the TSϕ its two best tracks serially in two consecutive bxs, ordered in quality. In order to minimize the latency of TRACO-TSϕ system, the TRACOs send Previews of track segments. While the TSϕ makes its selection (in pipeline), the TRACOs compute the full track parameters (absolute coordinates with higher precision). The TSϕ then serially reads the full track parameters of the two best tracks from the corresponding TRACOs, and sends them to the Sector Collector. With this mechanism 2 bxs are gained and the total latency of the TRACO-TSϕ system is limited to 6 bxs.

We define *bunch1* and *bunch2* respectively the first and the second bunch of tracks arriving from the TRACOs connected to the TSϕ. The sorting algorithm could be simple if it was just selecting independently the best track of *bunch1* and the best one of *bunch2*. However, it is not assured that the best track of *bunch2* represents the second-best track among all *bunch1* and *bunch2* tracks. The TSϕ must sort the truly second-best track among all *bunch1* and *bunch2* tracks. In order to achieve this, the TSϕ selects, among the tracks of *bunch1*, the first-best-track (FBT) and the second-best-track (SBT). On the following bx, the search for the best is done among *bunch2* tracks and the SBT of previous bx (*carry*). Therefore the sorting algorithm is applied in pipeline at each bunch. In this way the truly two best tracks are found among all the possible tracks. For normal triggers, the TSϕ is able to sort the two best tracks within two bxs. In case of pile-up triggers, the TSϕ is able to provide to the Sector Collector at least the FBT data resulting from the sorting of *bunch1*. In case of two close muons, they likely produce two track segments in *bunch1* from different TRACOs in the same stations, which are correctly picked up by the TSϕ algorithm through the *carry*.

The TSϕ logic diagram is shown in Fig. 9.12. The selection algorithm uses a two layer cascade of processing units. This architecture has been chosen in order to minimize the number of logic cells within a unit and the amount of I/O between blocks[1]. In each unit, a parallel minimum and next-to-minimum search is performed over a small group of input words, using 2 by 2 fast 9-bits comparators. The full parallel approach guarantees a fixed time response, independent of the number of TRACOs in a station. Each unit of the first layer (TSS: Track Sorter Slave) processes

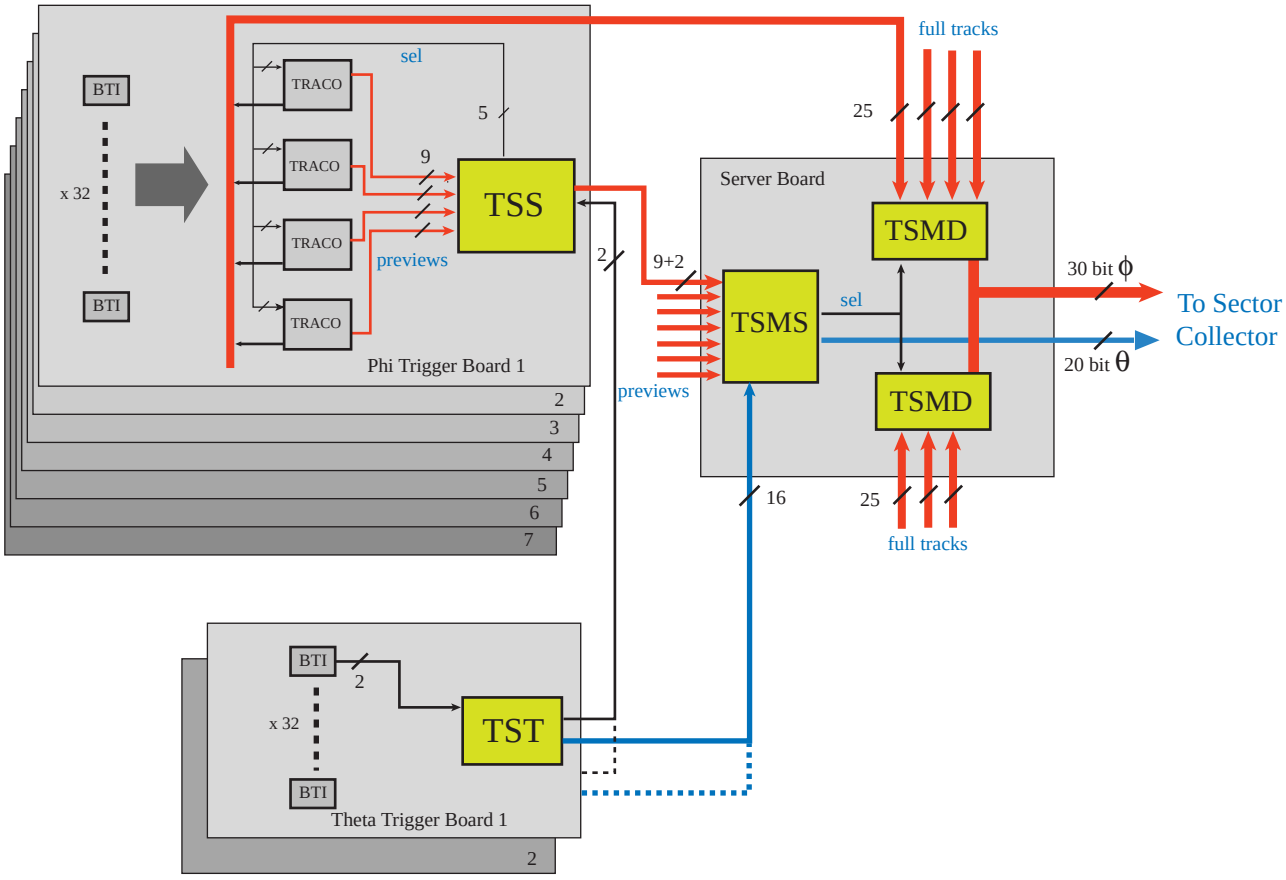


Fig. 9.12: Trigger Server architecture.

up to four data words, while the second layer unit (TSM: Track Sorter Master) processes up to seven data words.

The TSθ is formed by two identical units (TST), which form the OR of groups of BTIs: the information about the presence of a trigger in the θ view is sent to the TRACOs via the TSSs and can be used as trigger validation in the ϕ view. Besides a pattern of trigger hits is sent to the TSM and forwarded to the Sector Collector.

As shown in Fig. 9.12, the hardware partitioning of the system matches with the logical blocks. Each TSS device is mounted on a board (Phi Trigger Board) which contains 4 TRACOs and 32 BTIs. The TSM system is composed of three devices mounted on a separate board (Server Board) which receives the output of at most 7 TSSs (for the largest chamber). The two TST devices are mounted on two separate boards (Theta Trigger Boards).

The control and monitoring of the system is possible through a JTAG serial line which links the TSM, the TSSs, the TRACOs and BTIs. In case of failure of this link a backup solution is provided: a Parallel Interface which uses the lines normally dedicated for data transmission.

9.5.1 Track Sorter Slave (TSS)

The main tasks performed by the TSS [9.9] are the sorting of Preview data coming from the four TRACO placed on the same Phi Trigger Board and the suppression of noise generated by TRACOs.

The Preview consists of a 9-bits word: 4 bits are reserved for the quality of the track (First/ Second Track choice, H/L trigger, Correlation, Inner/Outer SL), the other 5 bits are used for the bending angle. The best track is the one with best quality and smallest angle (which means higher transverse momentum). If the quality bits are correctly coded, the search for the best track translates in search for the minimum. In one bx the TSS is able to activate a select line addressing the TRACO which sent the best Preview: the TRACO will send the corresponding full track parameters to the TSM for further processing. At the same time the best Preview is also sent to the TSM for the second stage processing.

There are two kinds of ghost segments that the TSS is able to recognize.

Due to the geometry of TRACO acceptance, a TRACO nearby to the TRACO that sends the best segments, can send a copy of the same track, which has to be an Outer segment. This kind of ghost can be canceled removing *carry* tracks of type Outer in the TRACO nearby the one that sent the best track.

If a TRACO cannot correlate two track segment in Inner and Outer SL belonging to the same track, it sends the Inner segment as a First Track the Outer one as a Second Track. This ghost can be removed by requiring that an Outer Second Track sent by the same TRACO which gave the best track in the previous bx, is not valid.

The final suppression of ghosts of the first type, which involves nearby TRACOs belonging to different Phi Trigger Boards, can only be done by the TSM.

From the point of view of controls and monitoring, the TSS contains the JTAG controller that can be addressed by the Controller from the Control Board: all TRACOs and BTI on the corresponding Phi Trigger Board are serially linked to the TSS.

The design of the device was done using the VHDL language, which guaranteed an easy portability on different hardware technologies.

Algorithm Description

The functionality of each TSS is performed in two consecutive cycles (one cycle per bx), called *sort1* and *sort2*. The *sort1* processing status is recognized when at least one TRACO gives a non-null track of *bunch1* type, while the *sort2* status simply corresponds to the cycle following *sort1*. The *sort2* status can be aborted in case of pile up triggers. In the *sort1* cycle, each TSS unit analyses four Preview data words and transmits the minimum to the TSM unit in the second layer, while the next-to-minimum is stored locally and carried over to the *sort2* cycle. At the same time a local select is given in output to enable transmission of the full data from the selected TRACO to the TSM. In the *sort2* cycle, each TSS unit analyses the four input words of *bunch2* together with the carry word of the *sort1* cycle. In case the carry results the best trigger candidate in the *sort2* cycle, a post-select line is used to inform the TRACO that it has to transmit to the TSM its best track segment of previous cycle.

The timing of the information handshake between BTI-TST-TRACO-TSS-TSM is shown in Fig. 9.13.

By use of internal configuration registers, it is possible to steer the sorting algorithm:

- each of the input Previews from TRACOs can be masked in case of noisy channels (it is also possible to mask only the tracks with a certain quality, for example only LTRGs).
- during normal operation the priorities used in the sorting are, in order of decreasing importance: correlation, quality of the trigger, position of the trigger (i.e. internal or external SL), angle deviation with respect to the radial direction. It is possible to swap the priority order of the quality bits.
- normally the carry track from s*ort1* cycle is used in *sort2* cycle: it is possible to disable this mechanism.
- it is also possible to disable the algorithms for ghost suppression.

Hardware Implementation

The TSS functionalities are implemented in a single 120-pin ASIC chip built in CMOS 0.5 µm technology. Because of the severe speed requirements (sort two out of four 9-bits words with carry in 1 bx) it is not possible to use programmable ASIC devices like it is done for the TSM.

The main building blocks of TSS are shown in Fig. 9.14:

Sorting core: it is the processing unit. The four 9 bits preview words from TRACOs are filtered: they can be masked individually or in base of their quality and the priority of their quality for the sorting can be changed. Then they enter a battery of ten 2-words comparators together the carry track of previous cycle. The First Best Track is sent to the TSM while the Second Best Track is kept as carry. At the same time selects line to TRACOs are activated.

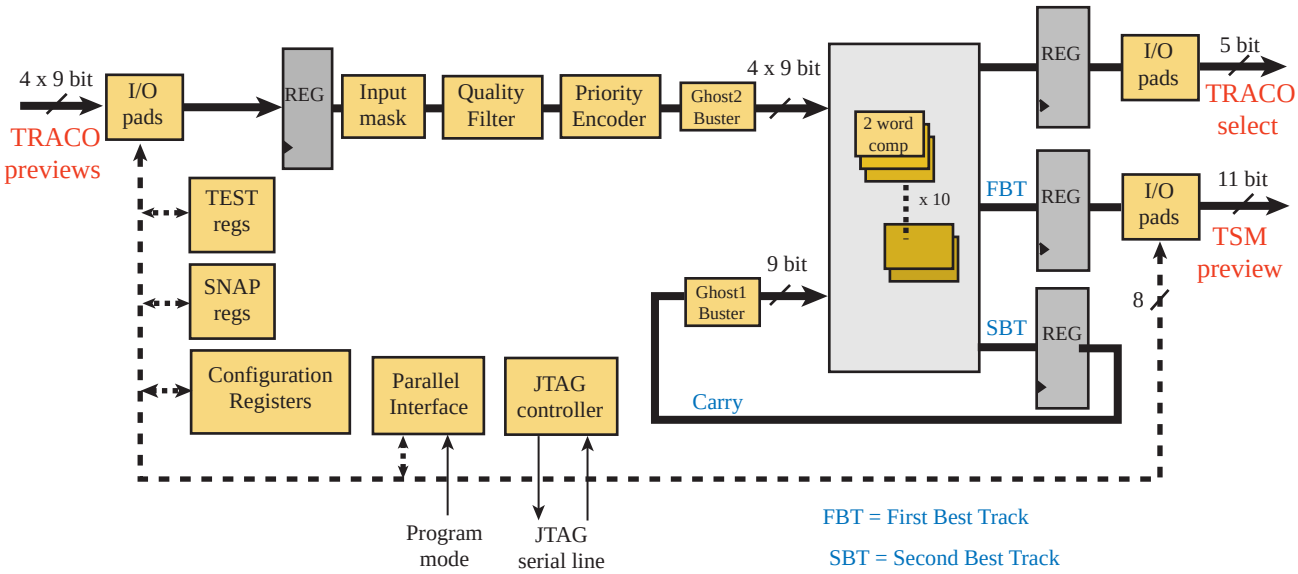


Fig. 9.14: Main blocks of TSS design.

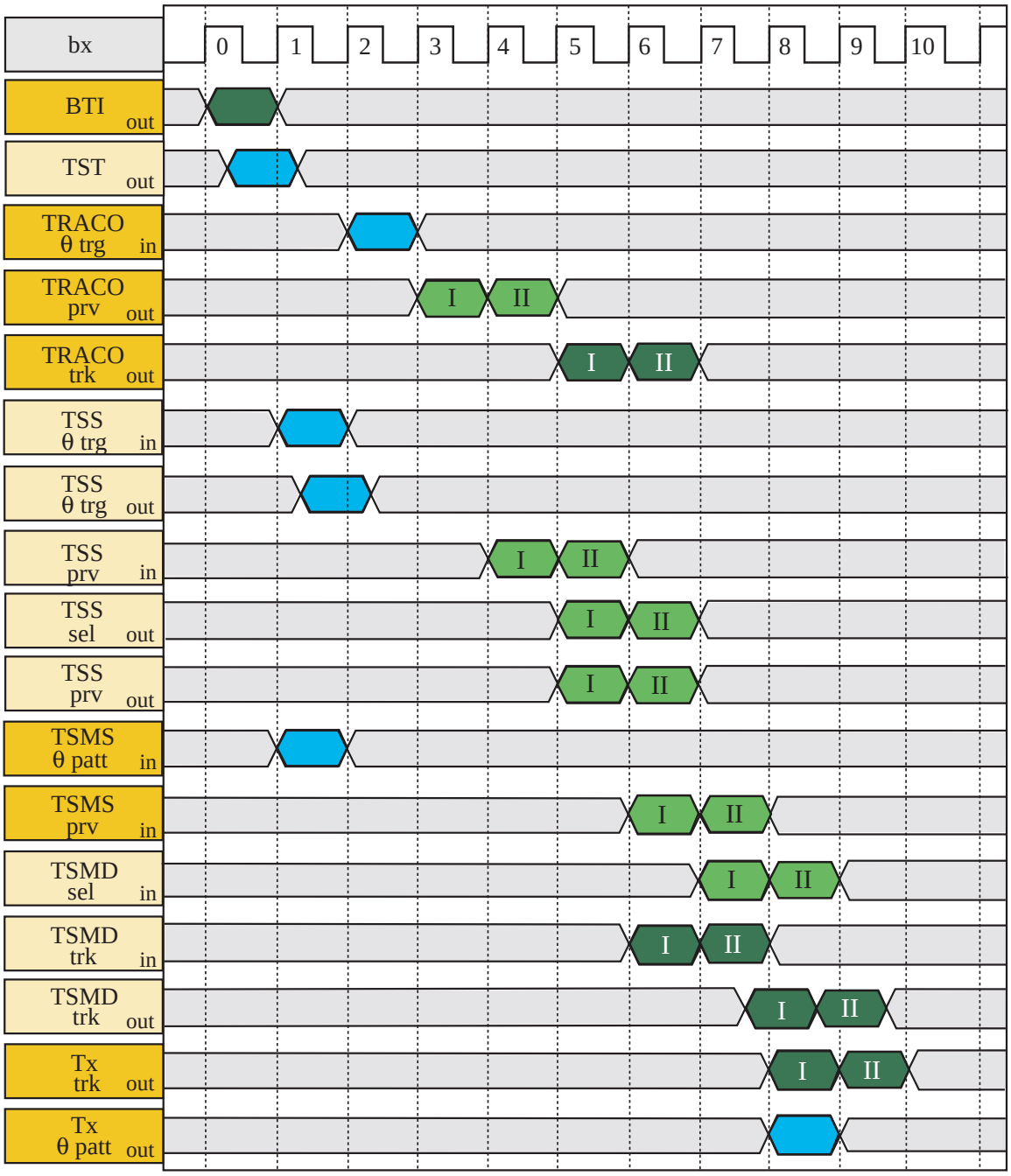


Fig. 9.13: TRACO-TS timing diagram. The sorting in the TSS is based on TRACO's previews (prv). The TRACO with the best track is addressed by the TSS through a select line (sel) and sends the full track parameters (trk) to TSMD. The second stage sorting in the TSMS is also based on previews sorted by the TSS. The two best tracks among the ones stored in the TSMD are selected by the TSMS (sel) and sent to the Sector Collector in two consecutive bunch crossings by transmitters (Tx). The information about the presence of triggers in the theta view (θ trg) is prepared by TST and, through the TSS, forwarded to TRACOs. The theta trigger hit pattern (θ pattern) is not used in the sorting and is forwarded to Sector Collector.

Configuration registers: it contains the seven 8 bits registers which are used to control the chip. They can be read and written through the JTAG or the Parallel Interface. With these registers it is possible to steer the sorting core and the filtering of input previews.

JTAG controller: it is the control unit for the standard JTAG circuitry. Besides the internal loop on I/O registers (Boundary Scan Registers) there are 3 user defined serial lines: for the Configuration registers, for Test registers and for Snap registers.

Parallel Interface Controller: this unit takes over the control of the bidirectional lines used for the Parallel Interface. After entering in program mode the sorting core is isolated. Eight bits of the preview word to TSM is used for communication with the higher level of Local Trigger architecture. Eight bits of each of the preview from TRACOs are used for communication with lower level devices. The direction of this bus is controlled in base of a protocol for read and write operations. Data can be read or written in configuration registers, test and snap registers in case the addressed device is the TSS itself, while in the other cases the bus acts as a bypass.

Test-in registers: these registers can be used in order to check the functioning of sorting core in offline mode. Patterns of preview words can be loaded into the registers by JTAG or Parallel interface. Then the patterns can be injected into the sorting core at 40 MHz.

Snap registers: the input and the output of the sorting core can be monitored. After the snap registers receive a reset they wait the first trigger condition (for example the presence of an high quality track among the input previews) after which the I/O are latched into flip-flops. These registers can be read during running time through the JTAG.

9.5.2 Track Sorter Master (TSM)

The TSM unit [9.10] in the second layer analyses up to seven Preview words from the TSSs. There is one TSM per Muon Drift Tubes Station. It behaves similarly to a TSS unit of the first processing layer, but its processing begins two bxs later. The information handshake between the TSϕ system and the TRACO devices allows data from up to fourteen tracks to be stored in the TSM unit. The selected output signal from the TSM, corresponding to the FBT in the first processing cycle and to the SBT in the second cycle, are used to enable the transmission of full track data to the Sector Collector for two out of the fourteen possible candidates stored in the TSM unit.

The TSM system has two different logic components (Fig. 9.15): a sorter block (TSMS) which performs the sorting on the Previews from the TSSs and a data multiplexing block (TSMD) which outputs the full data coming from TRACOs, corresponding to the selection done in the TSMS.

System robustness considerations, discussed further on, suggest to split TSMD into two hardware blocks, each one looking after half Muon DT Chamber and with the same functionalities and internal architectures. The TSMS, TSMD0 and TSMD1 are all placed on the Server Board

The TSM also receives information from the θ view. The hit pattern received from the TSθ is synchronized with ϕ view track data and forwarded to the Sector Collector.

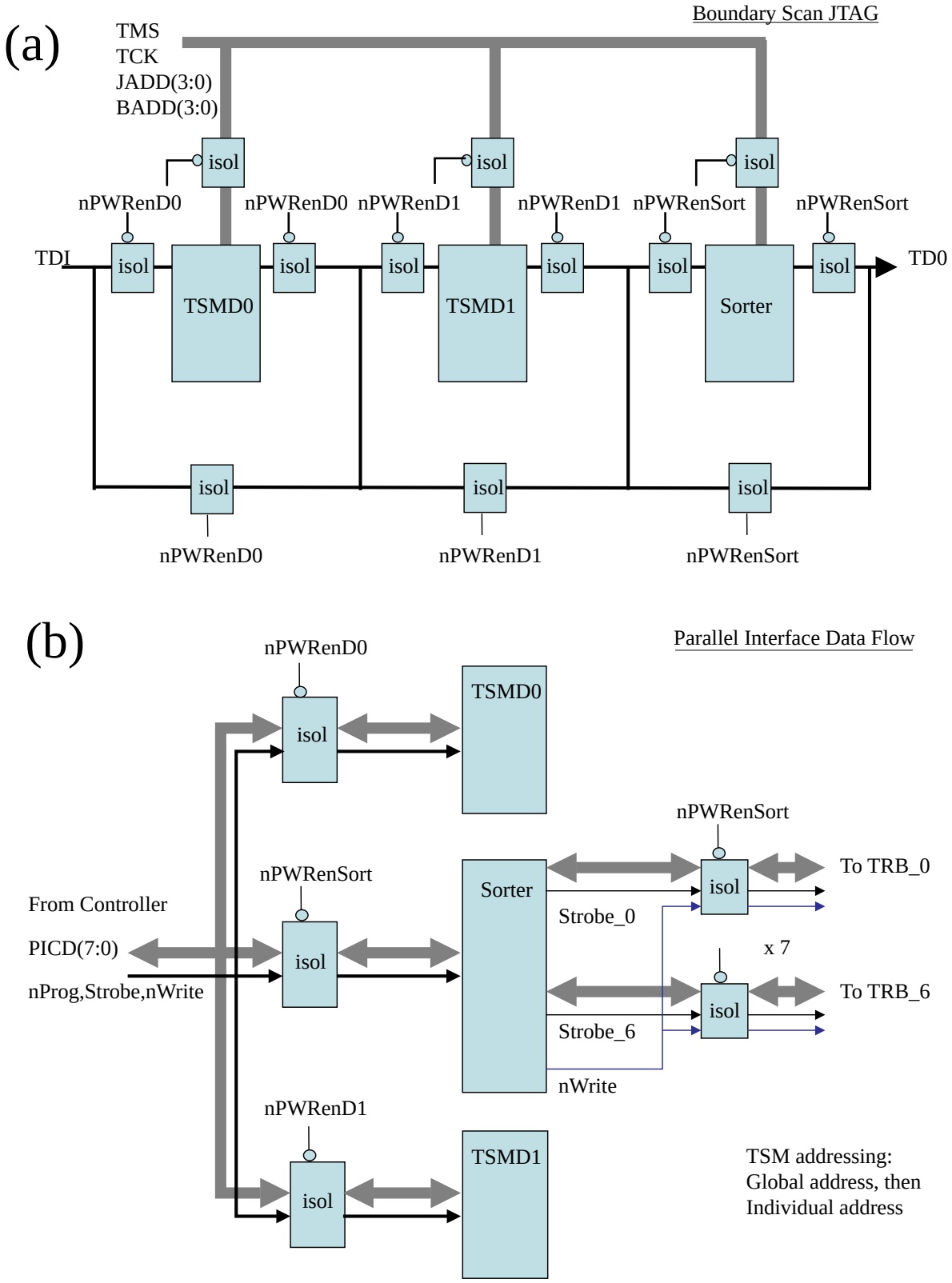


Fig. 9.15: The TSM system can be configured through both JTAG (a) and Parallel Interface (b).

Algorithm Description

The TSM is the last element of the TS system and of the muon on-chamber trigger electronics. Therefore a very important requirement in the TSM design is robustness. From the point of view of functionality, the main constraint comes from dimuon physics: this means capability of the system to maintain good efficiency also in case of hardware failures. To this end the system has been segmented in blocks with partially redundant functionalities. Care has been taken that the segmentation does not deteriorate the expected performance, in particular the latency assignment.

First the TSM is split into three parts: a TSMS block, two TSMD blocks (TSMD0,TSMD1). The TSMS has in input the Preview data from the TSSs. The TSMDs have in input the selected track candidates data for a half chamber each.

The TSM can be configured in two processing modes.

In the default processing mode the TSMS sorts on the TSS Preview data and issues select signals that the TSMDs use to choose between the track candidates coming from TRACOs. The TSMS can select two tracks in TSMD0 or two tracks in TSMD1 or one track each;

In the back-up processing mode TSMS processing is bypassed: each TSMD sorts the best track candidate among the data of a half chamber and outputs one track.

The default processing implements the full performance and guarantees that dimuons are found with uniform efficiency along the chamber.

In case of failure of one TSMD, the Previews of the corresponding half chamber are disabled in TSMS sorting, so that full efficiency is maintained in the remaining half chamber. Similarly in case of damage in the data lines from TRACOs.

The back-up processing is activated in case of TSMS failure or in case of damage in the Preview lines. It guarantees full efficiency for single muons and for open dimuon pairs (one track in each half-chamber).

Hardware Implementation

Robustness is the focal point in designing the TSM system, since TSM operates both as last functional element of the track-segment sorting tree of a DTBX chamber and as nodal point for distribution of the monitoring and configuring information to the many elements of the chamber local trigger.

Functionality is distributed over three ICs (TSMD0,TSMD1,TSMS) (Fig. 9.12) that can be configured in different processing modes, providing high redundancy in case of hardware failure. Each one has independent power lines. Three separate lines from the chamber Controller are used to provide enable signals (nPWRenD0, nPWRenD1, nPWRenSort) for the power switches. When one is powered down also all I/O lines to the chip are disconnected via switches driven with the power enable signals from the Controller.

Access to the configuration registers is possible in two ways: through a configurable JTAG net for boundary scan and through the DTBX ad-hoc configuration protocol, hereafter called Parallel Interface (PI). Fig. 9.15(a) shows the JTAG path through the three chips: the path adapts to run through the chips that are powered on, using switches controlled via the power enable lines. Fig. 9.15(b) shows how the PI bus lines are distributed through the TSM system; each individual

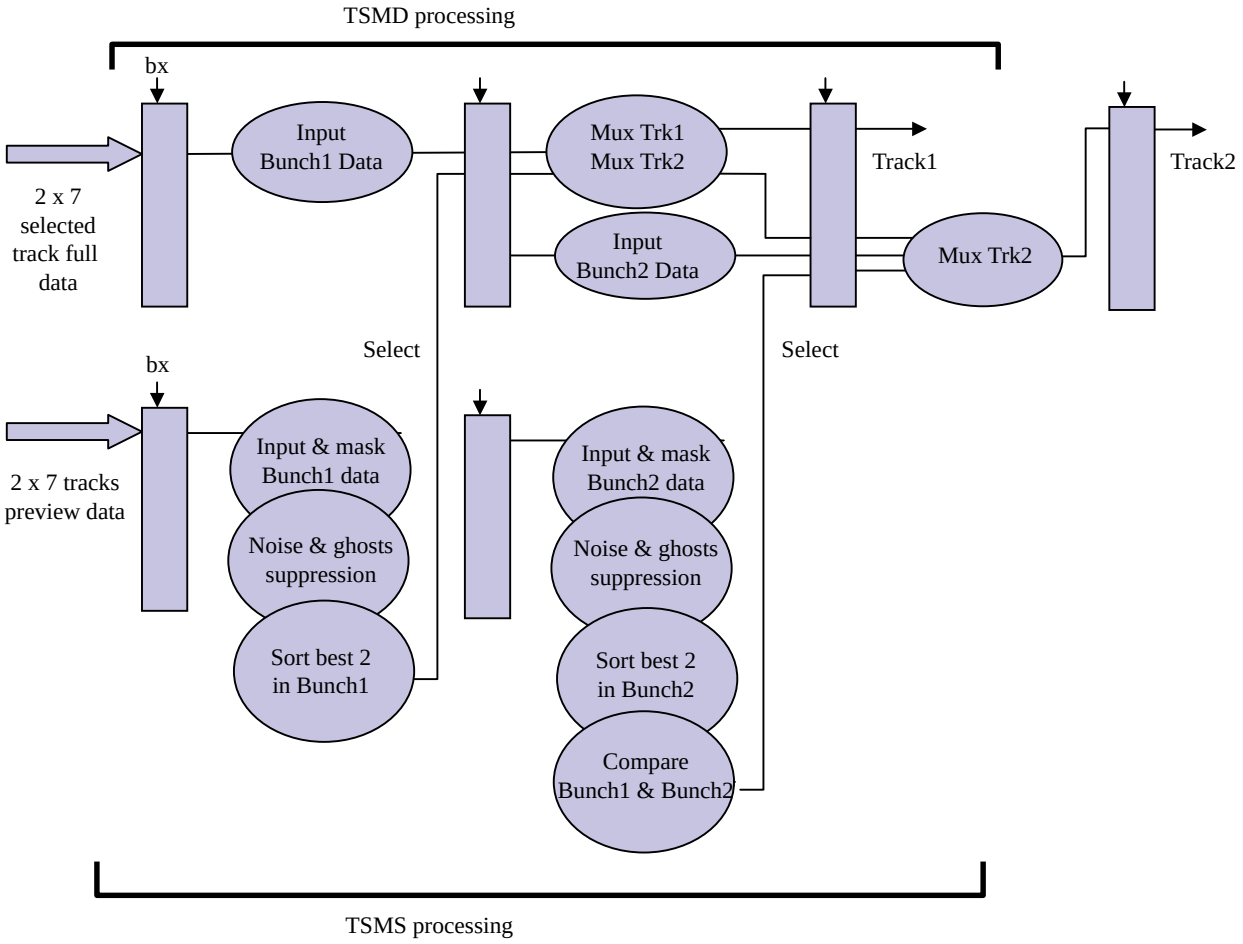


Fig. 9.16: Time sequence of TSM operations when in Default Processing Mode.

chip has both a common TSM address and its own address. The PI commands are forwarded to the trigger boards through only the TSMS which gives access to only one trigger board at once. In case of TSMS failure the trigger boards can be configured via their individual JTAG nets. The PI utilizes the same lines used for propagating the data whose direction is reversed during a PI writing operation.

The TSM configuration can also be changed from the chamber Controller by acting directly on the power enable signals: TSMS receives the power enable state of TSMD0 and TSMD1 and can it change its processing mode to select two tracks from the same TSMD, i.e. from half a chamber, when the other TSMD is powered off. Similarly each TSMD receives the power enable state of both TSMS and the other TSMD, and it switches to the back-up processing mode when the TSMS is not powered. The system can still run in the limit scenario of only one TSMD block and its connections undamaged. Three power fault signals are generated and reported to the Controller when an overcurrent condition is detected in the corresponding power net.

There are two main processing modes. The sequence of processing operations performed in Default Mode are illustrated in Fig. 9.16.

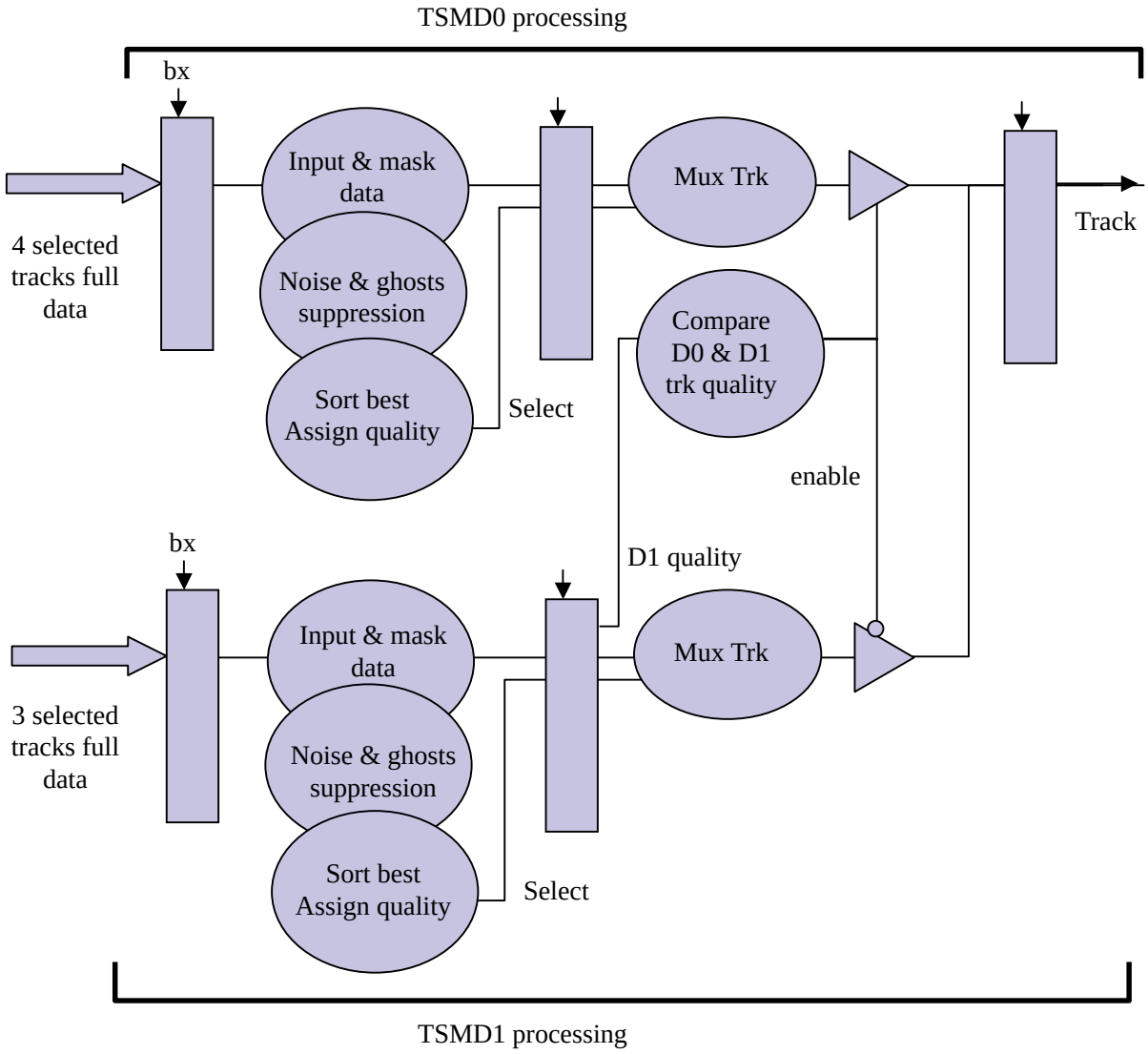


Fig. 9.17: Time sequence of TSM operations when in Back-up Processing Mode.

Two tracks, one per clock cycle, are presented on output on the same bus. The track selection is performed by the TSMS which applies the second stage of the sorting algorithm on the reduced data already processed by the TSS during the first sorting stage. The addresses of the selected tracks are used to drive the multiplexers of the data pipelined in the TSMDs and to enable the three-state output buffers of the TSMDs. The sequence of processing operations performed in Back-up Mode are illustrated in Fig. 9.17.

In this mode the TSMS is bypassed and each TSMD sorts the best track in half chamber data. The selection is performed on the full-track data from the TRACOs selected by the TSSs during the first stage of sorting. The quality (3 bits) of the selected track in TSMD1 is compared to the one in TSMD0 for enabling the corresponding three-state buffer on output. One track is output per clock cycle.

Besides performing the second stage of the sorting algorithm initiated in the TSSs, the track selection procedure also applies data masking, ghosts and fakes rejection, in a consistent manner to the TRACO-TSS system. In the TSM, ghost rejection is expanded to a new kind of ghosts: a single good track that produces two segments, one each in two neighbouring TRACOs, which then forward their segments to two different, although contiguous, TSSs. Both segments appear at the TSM input. To this end, since each TSS serves four TRACOs and this particular kind of ghosts can only appear in two contiguous TRACOs, each TSS forwards to the TSM two bits giving the relative address of the selected TRACO. The TRACO with address 00 of the TSSi is adjacent to the TRACO with address 11 of the TSSi-1. If such adjacent segments are found, one is cancelled if it is an OUTER segment, i.e. a segment only observed in the outer SuperLayer: no duplication of inner SuperLayer segments is possible in the TRACOs by construction.

The TSMD0, TSMD1, TSMS logic is implemented using three identical Actel A54SX32 chips, which, tested for space applications, have shown good tolerance to high radiation doses up to 10 to 50 krads and high thresholds for Single Event Effects (for instance 7 to 10 MeV cm^2/mg for SEU). They belong to a new generation of FPGAs also called pASICs (programmable ASICs) based on the 0.35 μm silicon antifuse technology: once programmed the chip configuration becomes permanent, making them effectively ASICs.

9.5.3 Trigger Server in the Longitudinal View (TSθ)

Theta Trigger Server has to group information from the 64 BTIs in θ-layer and to send an opportune pattern to the Regional Trigger. Studies on the Regional Muon Trigger [9.8] suggest that the minimum pattern resolution, without loss of efficiency in Track Finder reconstruction, correspond to the space covered by eight BTIs.

TSθ receives 2 bit from each BTI (trigger strobe and H/L quality) and, for both bits, it performs a logic OR of groups of 8 BTIs. The output is formed by 2 bits for each group: in total 8 bits for the trigger pattern plus 8 bits for corresponding quality. These signals are sent to the Server Board where they are synchronized with the track segments found in the ϕ view and sent to Sector Collector, which transmits them to the Regional Muon Trigger.

Moreover TSθ sends a 2-bit signal (64 BTI wired OR + 64 BTI Quality wired OR) to the TSSs, where they are forwarded to the TRACOs to help in noise reduction.

TSθ is made of two identical devices (TST). Each device is located on the Theta Trigger Board and connected to 32 BTI. TSTs are built using commercial ICs.

9.6 Sector Collector

The Sector Collector Board (SCB) is lodged in the mini-crate of the fourth station of each sector. All high speed optical links either for readout or for trigger are placed on the SCB. Readout data, coming from each Readout Board on serial medium speed links on twisted pairs, are grouped and formatted to form sector readout packets and sent, via a high speed optical ink, to the DAQ.

Trigger data, coming from each Server Board on high speed LVDS serial links, are grouped to form sector trigger packets and sent, via high speed optical links, to the Regional Muon Trigger (Fig. 9.18).

The link connecting each SB to the SCB consist of 48-bit LVDS Channel Link Serializer and Deserializer connected by a variable length flat cable with 10 twisted pairs. The device 48 inputs are latched at 40MHz and serialized on 8 twisted pairs at 240Mbit/s; one twisted pair is reserved for clock transmission. The different cable lengths (2m to 4m) compensate, within 2ns, for the different time of flight of particles coming from the vertex and crossing the sector stations. Sector trigger data amount to 164 bits and are transmitted to the Regional Muon Trigger using two PAROLI (Siemens) optical links, one for trigger ϕ view information and one for θ view information.

A new Sector Collector layout is under study aiming to move the unit out of MC electronics on the balconies. This option should allow relaxing device dimensions, power consumption and reliability requirements on trigger optical links due to bigger available space and easier access and maintenance. For this new setup, trigger cables from DTCCBs to SCB are much longer and a new transmitter based on LVDS serializers is under test. The possibility to replace the PAROLI optical link with a custom one using a VCSEL array is being evaluated. The seven Collector Boards of each half wheel are hosted in a crate together with a Drift Tubes Wheel Control Board (DTWCB). The DTWCB has two serial interfaces, one (called DTCI) is intended for test purposes only and one (called DTC1) is used for Detector Control access. Another connector (called DTC2) is provided, for the termination of the RS-485 link connecting all the DTCCBs of the half wheel. The DTCI is a standard RS-232 running at 9600 baud rate. The DTC1 is an asynchronous serial communication interface with optical connection for full duplex communication between the DTCM crate, sitting in counting room and balcony crate electronics. A total number of 10 optical links are needed to control electronics lodged on balcony crates.

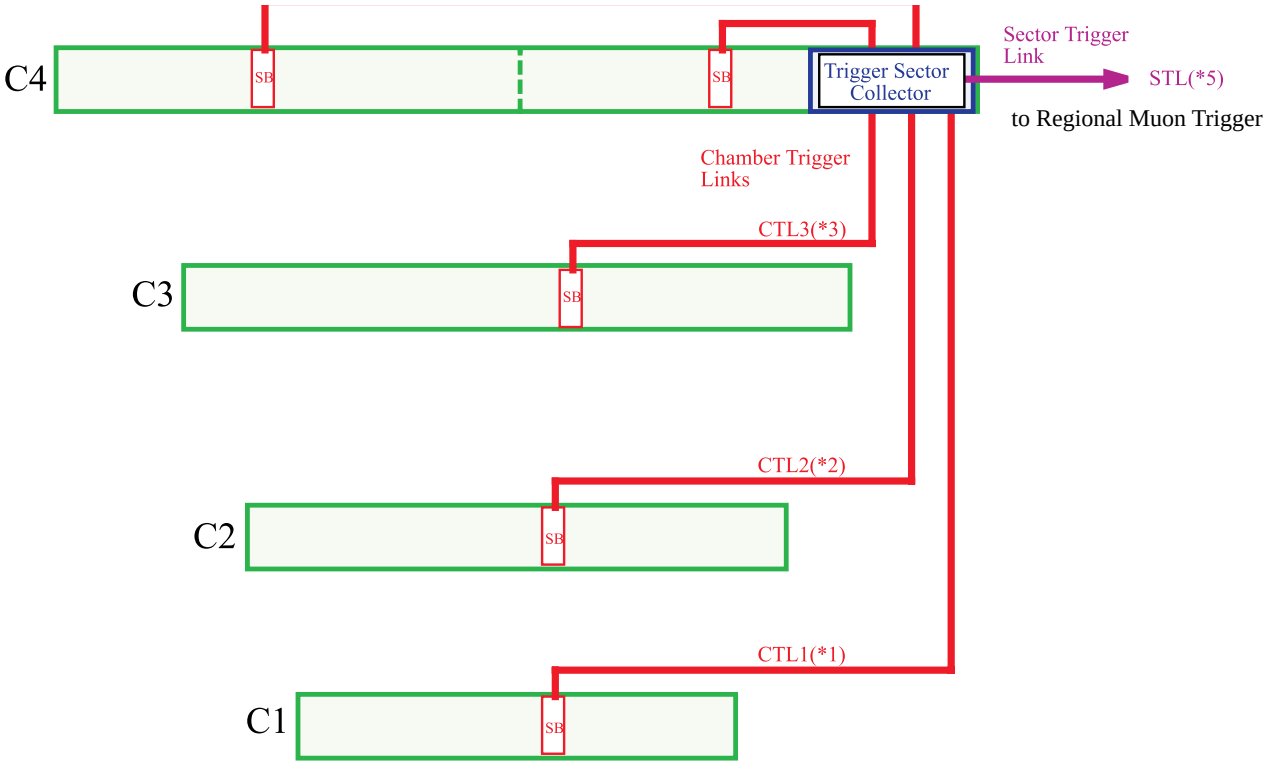


Fig. 9.18: Sketch of SCB connections to Mini-Crate electronics.

Table 9.2: Summary of standard data forwarded to Regional Muon Trigger from each muon chamber station

	Quantity	**# of bits**
ϕ-view	ϕ	12
	ϕ_b	10
	Quality	3
	I/II track flag	1
	Overlap	1
	Associated θ-view information	2
	Calibration flag	1
θ-view	Position	8
	Quality	8
	Associated ϕ-view information	2
	Synchronization control	2

9.6.1 Data Exchange with Regional Muon Trigger

The data will be packed inside the SC and sent to Regional Muon Trigger on an optical link for the ϕ-view information of each sector multiplexing First and Second Track data and with one optical link for the θ-view information.

The details of the data sent to Regional Muon trigger from each station are collected in Table 9.2. The data collected here are the ones sent form a standard station. Actually there will be some differences between stations: in fact θ-view layers are not available in station 4 and ϕ_b information from station 3 is not needed from the Regional Muon Trigger.

Taking these particular situations in consideration the link in the ϕ-view will send 110 bits per sector and the link of the θ-view will send 60 bits per sector.

9.7 Chamber Electronics Control System

9.7.1 Drift Tubes Control Interface

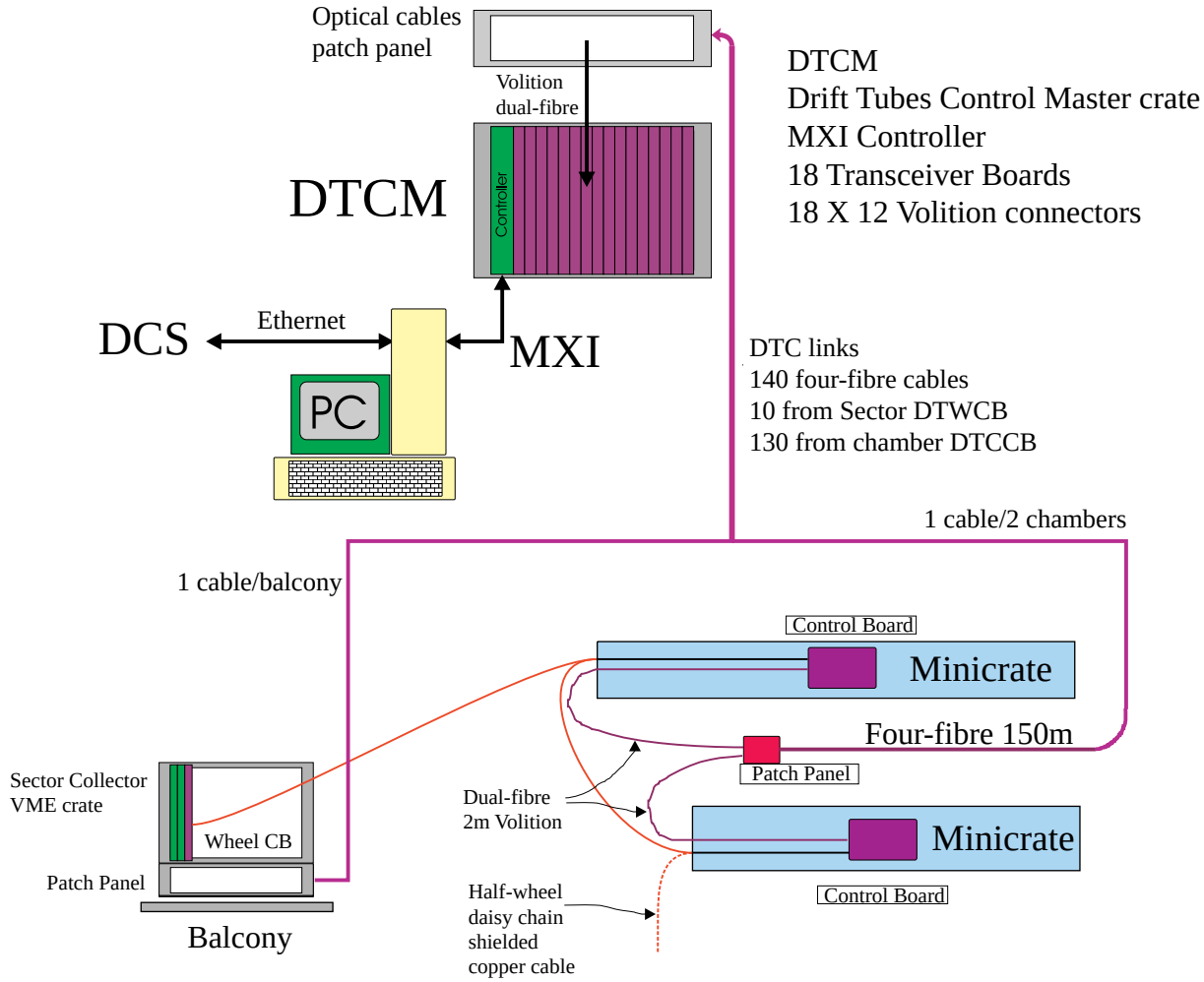
The Drift Tubes Control Master (DTCM), directly interfaced to the Detector Control System, interacts with each Control Board via a dedicated optical asynchronous serial bus called DTC1 (Fig. 9.19). A fiber pair per chamber is needed to communicate with the relative DTCCB. For budget reasons DTC1 lines are grouped in cables of four fibers. Patch panels are foreseen both

close to the drift chambers and at the DTCM crate in counting room. Patch panels consist of small boxes that, on the chamber side, are mounted on the iron between stations 1 and 2 and between station 3 and 4 to service the respective chambers.

An additional RS-485 connection, called DTC2 is foreseen as detector control backup in case of failure of the optical one. The DTC2 line connects in parallel all chambers in each half wheel and is serviced by a DTWCB sitting on the balconies. The ten DTWCBs are connected with dedicated optical fibers to the DTCM crate consisting of 17 Receiver Boards interfaced to a host PC via MXI bus. The connection between the DTCM and the Detector Control System is done via ethernet interface.

9.7.2 Control Board

The Control Board, as part of the Drift Tubes Control Unit, accomplishes control and monitoring functions of mini-crate electronics: a pictorial views of chamber Control Board is



Drift Tubes Control protocol is RS232 full-duplex

Fig. 9.19: Layout of DTbx Control System.

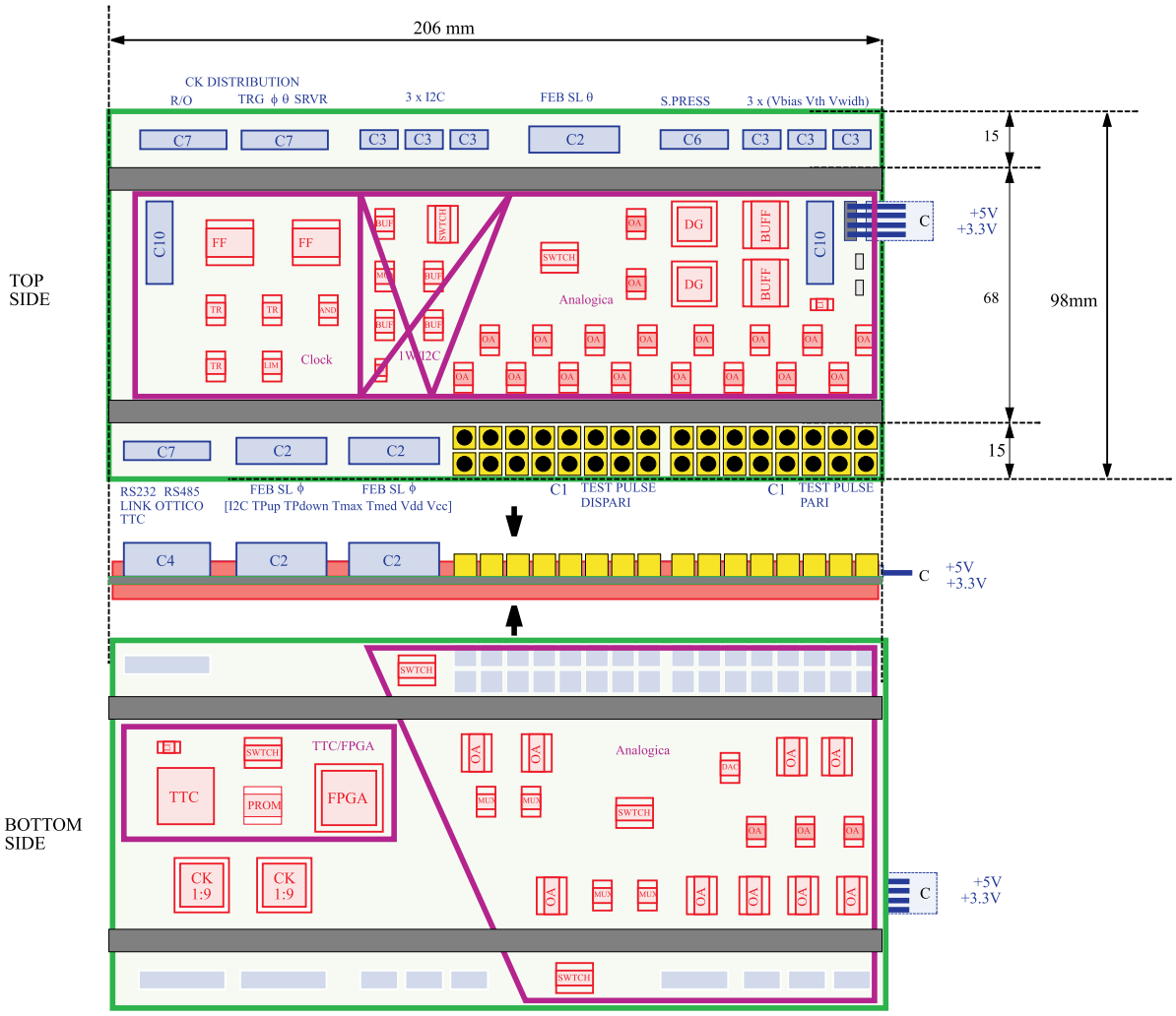


Fig. 9.20: Sketch of Drift Tubes Control Unit layout, the Control Board of DTbx mini-crate electronics.

shown in Fig. 9.20. Part of the control electronics is lodged on the Server Board of Fig. 9.6. A block scheme of the control system is reported in Fig. 9.21.

An on board microprocessor has access, either via JTAG or via a parallel interface, to all ASIC configuration registers. The chamber TTC receiver, used as clock and broadcast commands source, is located on the DTCCB. DTCCB functionality can be grouped in different units: clock distribution, test pulse, front-end analog signals, detector control interfaces, temperature measurement, power supply distribution and microprocessor unit (µPU).

Clock distribution logic consist of three blocks of Pseudo-ECL buffers delivering dedicated low skew clock lines for Trigger Boards, Readout Boards and Server Board. Each block can be independently enabled or disabled by the µPU. Clock cables consist of twisted pairs cut precisely in order to guarantee the same sampling clock phase at BTI inputs for all the three Superlayers.

The Test Pulse unit is able to inject a fixed and repeatable amount of charge into front-end inputs at the reception of a defined command. Furthermore, programming the unit is possible to

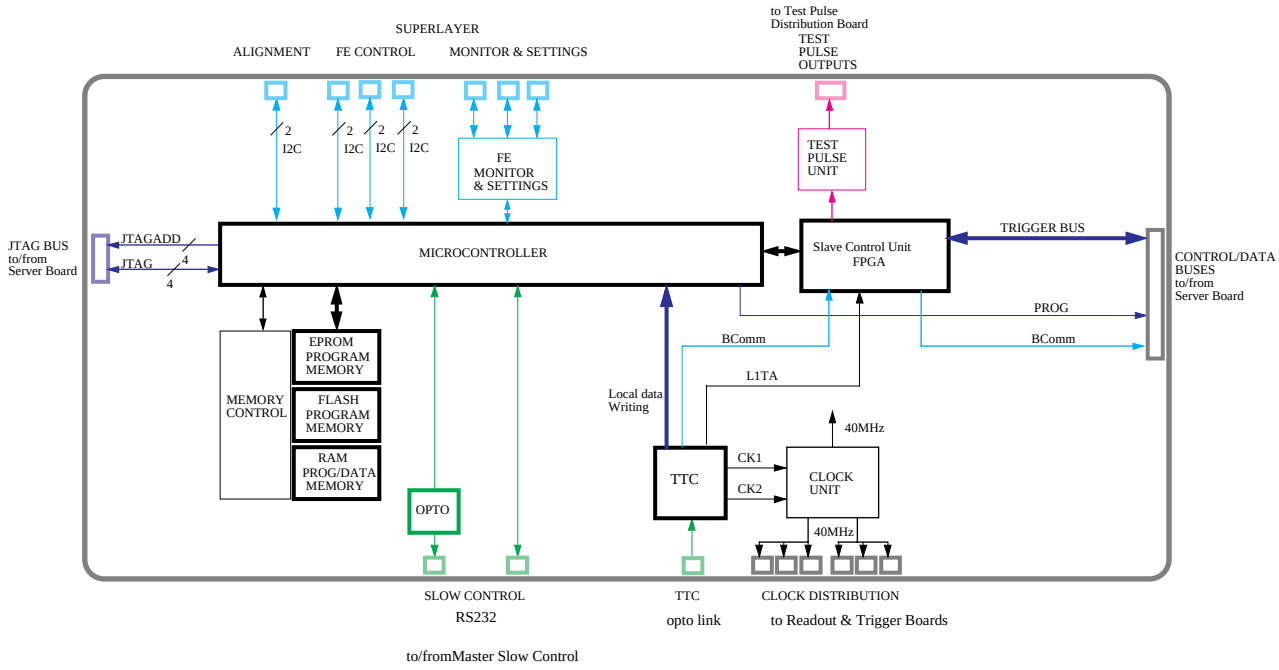


Fig. 9.21: Chamber control system block scheme

simulate a track normal to the Superlayer and crossing it at any position with 10mm resolution, allowing a precise characterization of TDC and BTI-TRACO performance. In order to reduce the amount of calibration data, charge injection is masked either at front-end output or at Readout Board input, limiting the number of hit channels to 4 per Trigger and Readout Boards. A description of the calibration sequence can be found in [9.11].

Front-end chips, called Multiple Amplifier and Discriminator (MAD) integrate all channel analog processing functions: amplification, discrimination and signal cable driving. MAD chips add new possible features to front-end electronics: input channels can be singularly enabled at the shaper stage, also an integrated temperature probe can be used for monitoring purpose.

Front-end electronics monitoring performs temperature and power supply measurements. Two temperature channels are provided with maximum and medium temperatures measured in MAD chips by dedicated cells. For external temperature measurements a large number of chips can be connected to the Control Board temperature connector for a maximum of 300m cable length.

Control Board access is guaranteed by means of three serial interfaces, one intended for test purposes (called DTCI) only and two for the detector control, as main (called DTC1) and back-up (called DTC2) accesses.

Three I2C buses are provided dedicated to front-end, RPC and alignment electronics programming.

Readout and Trigger ASICs are programmed via JTAG. As already mentioned every Trigger and Readout Board has a JTAG chain useful for unit setting and testing. Boards can be accessed one at a time by means of chain addressing. Four lines are used to address a maximum number of 16 units. During normal operation mini-crate ASICs can be accessed for monitoring purposes without any interference with trigger and readout activity. To guarantee the capability to

configure all trigger devices a back-up channel has been provided for device programming. Using the trigger data path backwards all ASICs can be addressed by the Trigger Sorter Master once the µPU has taken control of the bus. A dedicated parallel interface between the µPU and the TSM has been implemented for this purpose.

At power supply turn-on every Control Board the µPU starts executing the reset sequence. The boot program, sitting in EPROM, is executed as soon as power voltage stabilizes at nominal value. This program takes care of first hardware diagnostics, checking FLASH and SRAM functionality and power supply bus-bar voltages. After the self-check the result is sent via detector control link and the µPU enters a sleep state waiting for remote commands. At this level it is possible to turn on and off any block, to repeat the boot sequence and to access FLASH and SRAM memories for program downloading and execution. Standard program execution foresees the copy of code from FLASH to SRAM and FLASH memory power off for code source protection from SEE. Program execution can take place either in FLASH or in SRAM memory blocks; a separate power supply line allows an independent use of both. On top of program execution a progressive power on sequence is foreseen to allow a full check of mini-crate electronics integrity.

A TTC receiver per mini-crate accomplishes clock and broadcast signals distribution over the barrel drift tubes detector. Every TTC receiver chip delivers two clock lines with programmable fine de-skewing: one is distributed to all Trigger and Readout Boards while the second is used by Server and Control Boards. TTC programming is done via an I2C interface.

9.8 Synchronization and Latency

9.8.1 Synchronization Procedure

Description of the Muon Barrel Signal Path

The first issue of a synchronization procedure [9.11] is the definition of the basic block whose phase adjustment is done by hardware construction, assuring the synchronization with a careful compensation of the known delays. This compensation can be hardware achieved only if there are short electrical connections between the components of the trigger/readout chain and it requires the knowledge of all the contributions to the delays.

All the local trigger and readout electronics is lodged on the chamber itself; therefore it is sensible to believe that every chamber could be considered an intrinsically synchronous block, equipped with one Trigger Timing and Control Receiver (TTCrx).

The internal timing distribution is equalized using cable connections of adequate length and the maximum skew between internal parts is foreseen to be below 1ns. The trigger and readout data are sent to the Sector Collector (SC) lodged in station 4 using differential signals on twisted pair cables. Trigger cable lengths are used to compensate the difference in time of flight of the four stations of the sector in order to synchronize the full sector data at the trigger optical link input. Fig. 9.22 gives the time of flight and cable delays for each station within the same sector; once stations are synchronized with the beam the data skew at the SC input is within 3ns (cfr Table 9.3).

The TTCrx of each station provides two clocks with independent phase adjustment: one is used as sampling clock while the other is the data transmission clock (see Fig. 9.23). The first one is distributed, using equalized cables, to the chamber trigger and readout front-end ASICs. Its

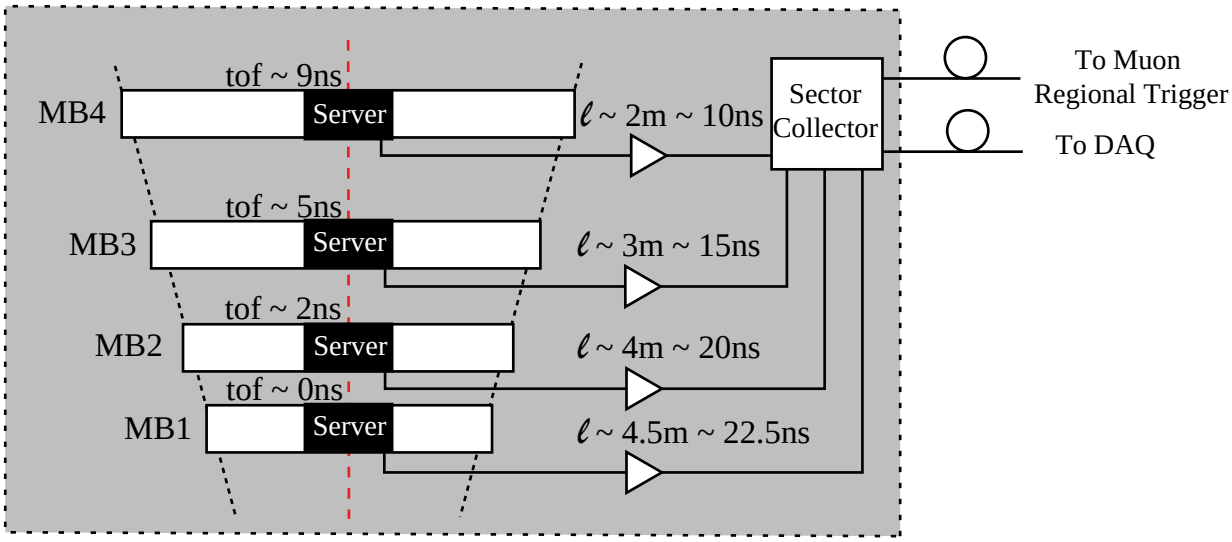


Fig. 9.22: Time of flight and cable delays to the Sector Collector in the Central wheel.

phase has to be set to compensate the time of flight to assure the highest trigger efficiency averaged on the chamber. The transmission clock phase has to compensate for the internal difference (less than 5ns) of signal propagation in order to align the data at the Trigger Server for the transmission to the Sector Collector. The time difference between the two clocks is a constant value determined by the hardware layout and set before chamber installation. This difference will be measured on the bench: hence only the sampling clock phase needs to be evaluated online.

Sampling Clock Synchronization

This is the first procedure to run because both the chamber trigger efficiency and the coherence of trigger data transmitted by the Sector Collector unit are strongly dependent on sampling/transmission clock phase.

This procedure is executed on the monitor CPUs in the control room in parallel for all the chambers. A special single station LV1A is generated by the drift tubes trigger system every time there is a very High Quality Trigger (HH or HL or LH) inside any station. Since many triggers will

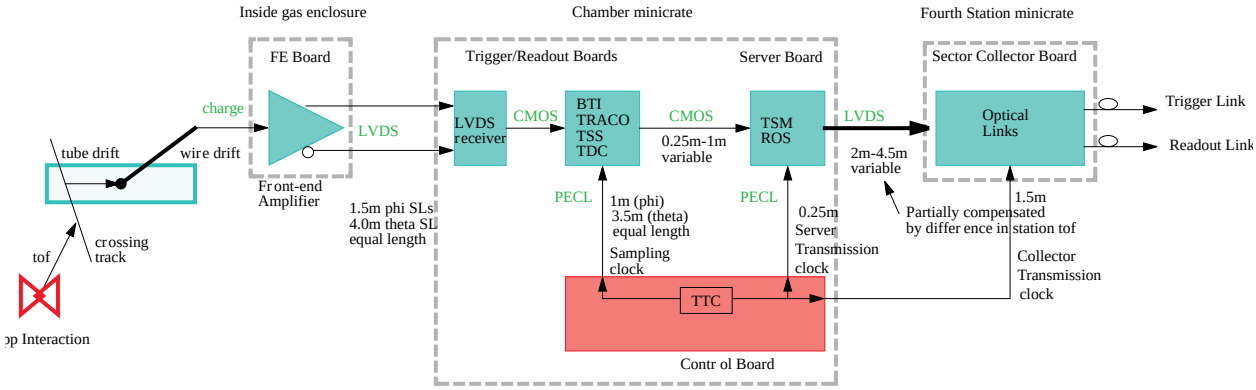


Fig. 9.23: Block diagram of the signal path in the muon electronics.

be available a the same time, they can hide each other: the procedure is therefore repeated disabling the chambers already aligned until they are all synchronized.

We take advantage from the synchronous nature of the trigger electronics. A trigger can be generated only at 40 MHz frequency, hence in the case of a bad synchronization a certain fraction of them will be assigned to the time slots close to the right one.

For every trigger the TDC data are readout from the FIFO and since they are triggered by the BTI itself, they will carry the offset introduced by the actual time slot assignment. Once the triggering BTI is identified, the drift times of any three consecutive layers are used to compute the quantity $T_1+2T_2+T_3$; histograms of this quantity are accumulated. The value depends on the trigger latency, and indirectly, on the sampling clock phase: if the sampling clock is out of phase

Table 9.3: Average delay and maximum spread due to muon time of flight and signal propagation along the wire at the electronics lodging position for each muon chamber.

Chamber	Average delay (ns)	Spread (ns)
MB/2/1	27.3	1.2
MB/2/2	29.3	1.5
MB/2/3	31.9	1.8
MB/2/4	34.6	2.0
MB/1/1	21.6	2.3
MB/1/2	24.1	2.6
MB/1/3	27.3	2.9
MB/1/4	30.5	3.1
MB/0/1	19.0	4.3
MB/0/2	21.9	4.4
MB/0/3	25.4	4.4
MB/0/4	28.8	4.4

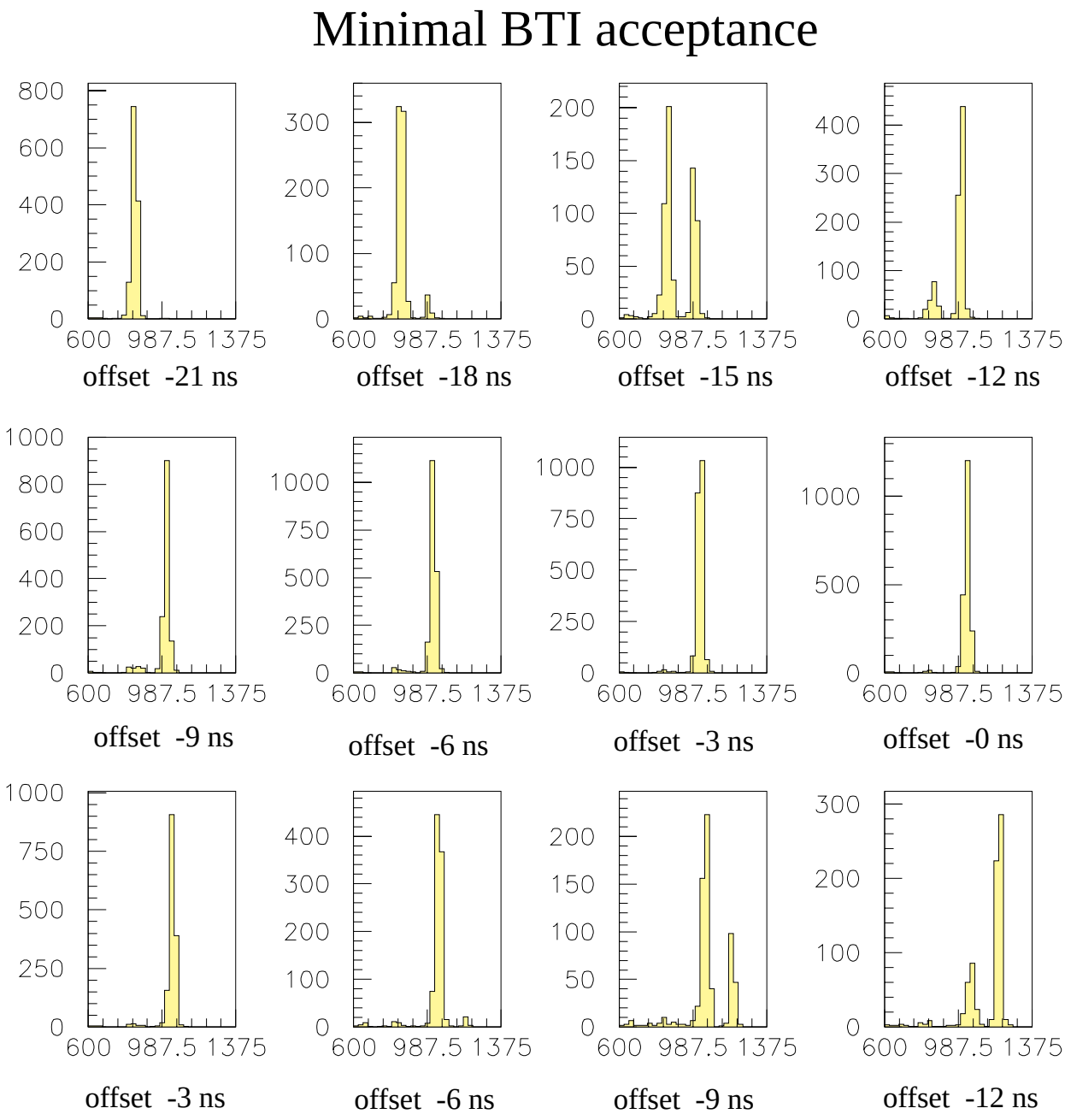


Fig. 9.24: Distribution of the quantity $T_1+2T_2+T_3$ for different synchronization offsets and minimal BTI acceptance.

the BTI is not able to identify uniquely the track crossing time and the trigger output is distributed over two neighbouring cycles; as a consequence the distribution shows two distinct peaks.

Fig. 9.24 shows the distribution of this quantity for a set of simulated data in the case of minimal acceptance to enhance the effect. The oscillation between two peaks and one peak histogram is quite evident. It is not sensible to look for this behavior and visually establish the best synchronization time. We have therefore to find an automatic algorithm. The easiest indicator is the r.m.s. of the distribution for each synchronization time set. The value of this quantity is plotted in Fig. 9.25 for the same sample and the same configurations we considered before: it shows a

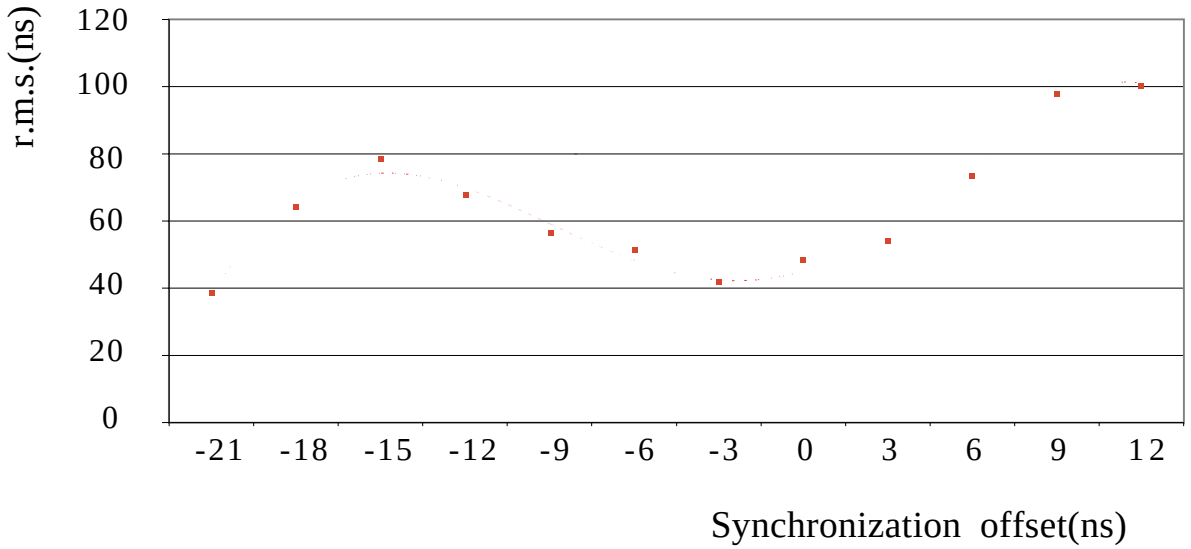


Fig. 9.25: Root mean square of the distribution of the quantity $T_1+2T_2+T_3$ for a simulated event sample as a function of synchronization offset for different BTI alignment tolerances.

rather evident minimum at the correct synchronization time. The r.m.s. method is safer than an equivalent rate counting method since it will not depend on eventual luminosity drop during the time required to run the procedure varying the synchronization time (roughly about 30 minutes at maximum luminosity for each iteration). This algorithm is sensitive only if the track incident angle is limited below 20˚: higher angles cause algorithm failures.

Hence the algorithm will store the histograms and find the right clock phase looking for the minimum of the root mean square value of the quantity $T_1+2T_2+T_3$. In order to have the highest possible resolution in this procedure the BTIs must be programmed to trigger with minimal acceptance, i.e. with half the standard alignment acceptance. With this setting the BTIs show a consistent efficiency drop when the clock phase is not correct. The TTCrx fine phase adjustment in changed with 3ns steps repeating the procedure and interpolating the results. This procedure is dependent neither on trigger rate nor on beam pattern.

Once the sampling clock phase is determined for each chamber, there may still be a difference between the various chambers quantized in steps of 25ns, when the data are sent to the SC.

TTC Links Synchronization

Once all the chambers are “in phase” with the beam it is possible to adjust the different TTCrx delays looking at the time distribution of local trigger events. Every time a local High Quality Trigger is detected its arrival time with respect to the BC0 is histogrammed. Once filled, the histogram is cross-correlated with the expected LHC beam pattern.

Trigger Links Synchronization

The trigger links are located in the SC unit: the transmission clock phase is fixed by hardware in order to be synchronized with the Server Board transmission clock. The different trigger link delays are compensated using FIFOs at the receiver end. Once TTCrx have been

synchronized the Test Pulse System (TPS) can be used to generate trigger data at the same time in all the chambers. The Regional Trigger should act on the trigger link receiver FIFOs in order to get the test pulse trigger data at the same time from all the SCs.

9.8.2 Latency Determination

Chamber trigger latency can be divided into three contributions: analog signal propagation, trigger computation and digital signal propagation as shown in Table 9.4.

Analog signal propagation consist of particle time of flight from interaction vertex to detector sensitive volume and detector signal propagation up to trigger front-end input.

Trigger computation is divided in BTI, TRACO, TSS and TSM parts, including synchronization time needed for detector asynchronous signals sampling. TRACO and TS computations overlap, reducing the sum of the respective latencies to 6 clock cycles: the actual computation time of each device is 6bx for TRACO, 6 bx for TSS and 3 bx for TSM.

Digital signal propagation includes data transmission from the Server Board to the Sector Collector and from the Sector Collector to the Regional Muon Trigger. Since synchronization of trigger links is accomplished in the Track Finder, using programmable depth FIFOs, length of sector links are at minimum and respective latency is intended as maximum.

Table 9.4: Drift Tube Chambers Trigger Latency

	Time (ns	bx cycles
Time of flight (4 to 10m)	33	
Cell drift time	380	
Wire signal	5	
Front-end electronics	3	
Cables front-end	20	
Total	441	18
BTI		4
TRACO-TSS-TSM		9
Chamber link		1
Sector Collector		2
Sector link		20
Total		54

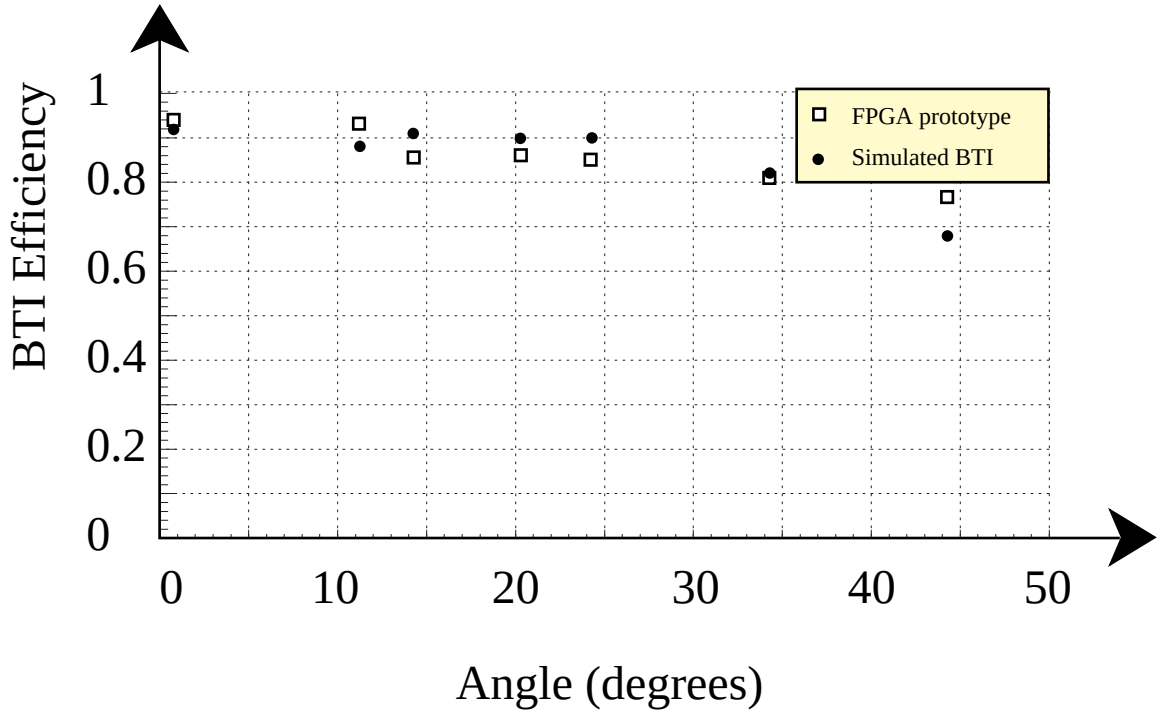


Fig. 9.26: Comparison of the measured efficiency versus the track inclination for the FPGA prototype and the BTI model with LTS.

9.9 Prototypes

9.9.1 BTI Prototype and Test Bench Performance

The first BTI prototype [9.12] [9.13] [9.14] was designed using FPGA technology, while the other prototypes where produced as custom ASIC chips.

Although using the biggest available FPGA at the time (XILINX XC4013, 6 ns grade) the implementation of the algorithm encountered serious space limitations, forcing us to downgrade the requirements.

We could build only a device programmable for fixed incidence angle including only a part of the wire couples and we could not output any information on position.,Three FPGA prototypes were tested on a chamber prototype. Efficiency and uniformity of the response were checked in order to tag eventual algorithm defects. As an example the average efficiency for different incident muon directions that could be extracted from the data is given in Fig. 9.26. The efficiency is compared with the expectation results of the Montecarlo used to tune up the prototype design and to define the sets of couples. The good agreement between Montecarlo and FPGA behaviour is a sign of the good quality of the trigger design, but the difficulty found to fit the needed logic blocks inside the FPGA demanded an ASIC device.

The ASIC prototype chip [9.15] was designed using the Standard Cell technique in a CMOS 0.5µm technology with three layers of metal. The total area was 19mm^2 for 60kgates and prototypes were packaged either in a ceramic 68 pins LCC or in a 68 pins plastic TQFP. The BTI,

when powered at 3.3V dissipates 200mW at 80MHz operating frequency. To get the best efficiency to noise ratio in the operating background conditions a careful setup is needed of programmable parameters like angular acceptance, time filters, drift velocity and wire dead time. The latency is equal to the maximum drift time (dependent on the programmed drift velocity) plus 100ns (8 clock cycles) for chip calculations.

BTIs can be programmed either via a JTAG (IEEE Std. 1149.1-1990) port or via a parallel interface using the trigger data bus for back-propagating parameters from TRACO and TS.

The JTAG port can be used either to check chip interconnections during the PCB verification or to program internal registers. A built-in feature of this interface is the capability to monitor chip activity without interfering with the trigger function. This can be performed accessing (via a SAMPLE instruction) the snap registers connected to the input signals and to the output bus.

The parallel interface, much faster than the JTAG one, can access all the BTI internal registers and is thought to be a backup solution for BTI setup. Using the trigger bus the downstream devices have the possibility to access the internal registers of the connected BTIs.

System testability and visibility are good owing to built-in self test logic, snap registers insertion and boundary scan implementation.

The BTI includes built-in self test logic (BIST) and emulation capabilities for testing purposes. In spite of the large input domain, chip validation can be performed using a set of 64k vectors only, thanks to the BIST circuitry.

Trigger diagnostics is possible using the BTI emulation mode. First the timing data of events to be tested are downloaded in the involved BTIs; then chips are programmed in emulation mode. When the specific trigger command is issued, the event is emulated at full speed and the relative trigger data can be found stored in the snap registers or can be directly read out with the programmed latency at the chip output.

The emulation mode was used to perform bench tests before using the BTI on a chamber prototype. The benchmark was composed by a 40K sample of hits generated using the full GEANT simulation of single muons in front of a BTI in order to have a realistic spectrum of the input data.

The efficiency as a function of the angle of incidence is reported in Fig. 9.27, showing that we have a flat response till 45°, while efficiency is rapidly falling till 55°, matching our design expectations.

9.9.2 TRACO Prototype and Test Bench Performance

TRACO prototypes have been designed as standard-cell ASICs using ATMEL 0.5mm CMOS technology with three metal layers. *Being currently tested.*

9.9.3 TSS Prototype and Test Bench Performance

The first preliminary studies of the sorting algorithm were done using an FPGA device which revealed the necessity to use an ASIC in order to fulfil the speed requirements.

A full performance prototype was built at the end of 1997 using 0.7 µm CMOS technology (two metal layers) [9.16]. The sorting is performed among four 10-bit words and the chip has all the functionalities necessary for the integration with the TRACOs and BTIs on the Phi Trigger

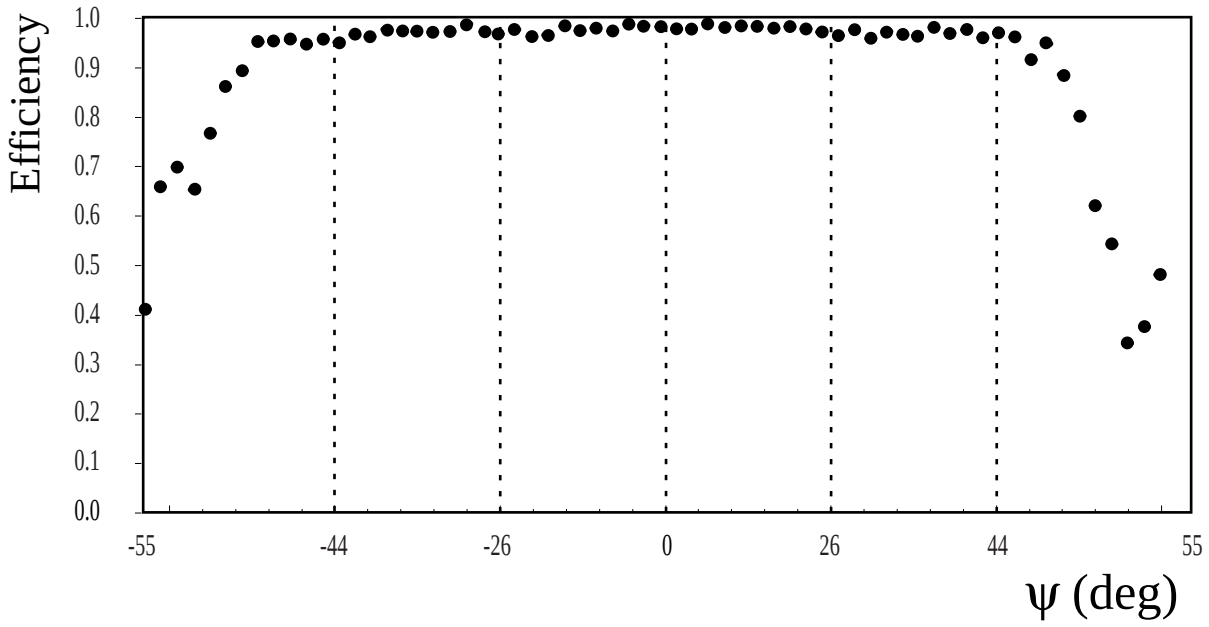


Fig. 9.27: Bunch crossing detection efficiency for a set of ASIC BTIs. The LTS mechanism is not active and notice that the abscissa scale is not linear.

Board. The area of the chip is about 23 mm^2 and is determined by the 104 I/O pads. Ten prototypes were packaged in ceramic 120 pin QFP. The TSS, powered at 5V, dissipates about 150 mW at 40 MHz.

The chip prototype was mounted on a test board and tested in standalone mode. Patterns were generated with a VME 40 MHz pattern generator, the Pattern Unit [9.17] [9.18], and injected into the TSS prototype using flat cables. The output of the chip was read back by the Pattern Unit. Sequence of test patterns were prepared with a software emulator with the same functionality implemented in the hardware and the output of the chip was crossed-checked with the expected result. In this way it was possible to test all the functionalities of the TSS. The chip was working up to 60 MHz. The final TSS chip will be produced using 0.5 μm CMOS technology with three metal layers and a significant improvement of the performance is expected.

9.9.4 TSM Prototype and Test Bench Performance

A prototype of the TSM system was built in 1999. The TSMS, TSMD0 and TSMD1 logic for the sorting functionality was implemented using three identical Quicklogic pASIC chips QL3025, speed grade 3, 208 pins. They were hosted on a prototype Server Board, with dimensions enlarged to fit in a VME 6U crate, which provided connections for the control signals and I/O (404 bits), and test points on all internal connections between the three chips. PREVIEWs and full-track data were generated at 40 MHz with three Pattern Unit [9.17] VME boards, mimicking seven Trigger Boards connected to the TSM system. Control signals were provided through a fourth Pattern Unit board mimicking the DT chamber Controller. A Pattern Unit with special adaptors with LVDS receivers was used to read the TSM output. In this prototype the two output data word, i.e. the two selected tracks in the chamber, were transmitted on two separate data busses in parallel in one clock cycle.

The system was tested using a set of about 1200 specific patterns, which, developed as case studies during the system design and simulation, test all the different aspects of the TSM sorting functionality. The TSM prototype successfully passed all the tests:

(i) the functionality of the individual chips was validated;

(ii) the propagation times to the chips, from the TSMS and the TSMDs, from the TSMDs to the LVDS output drivers were studied in detail and validated;

(iii) finally the system functionality was validated.

The TSMS sorter chip was also implemented and tested using a Actel A54SX16, which showed better performance than the Quicklogic chip.

9.10 Test and Simulation Results

The drift tubes local trigger will be implemented using special purpose devices. It was essential to have a simulation of these devices interfaced to the general CMS simulation in order to test the expected performance of the hardware and verify the algorithm effectiveness. Thus a very detailed simulation of the L1 muon trigger description was developed inside the CMSIM framework and is continuously maintained and updated to reflect hardware changes. Recently all the code was successfully translated in the OO technology inside the ORCA program [9.19].

The geometry of the muon chambers layout reflects always the latest available mechanical design, including dead areas. The digitization is performed on parametrized functions, (depending on impact position, crossing angle and B field components) obtained by detailed studies using the drift cells description program GARFIELD, whose predictions were verified on available situations real test beam results. The simulation includes all the known backgrounds (bremsstrahlung, δ-ray production,...), excluding pile-up from events on other bunch crossings. While the CMSIM simulation uses floating point calculations although taking care of integer bit rounding effect, the ORCA simulation is completely bitwise. Simulation results reported here refers either to CMSIM version 117 or to ORCA version 3.

Several test were done either on bench or in test beam areas or under cosmic rays on the available trigger electronics during the past years. The BTI prototype was in fact completely tested in several environmental conditions.

In the following paragraphs we will show the test results of the BTI prototypes and the behaviour expected from simulation of the other devices in the drift tubes trigger chain.

9.10.1 Bunch and Track Identifier

The BTI ASIC tests were performed at the CERN Gamma Irradiation Facility (GIF) in August 1998 exposing a full size chamber to a muon beam with energies in the range 80-100 GeV and during winter 1998-1999 in the Legnaro INFN National Laboratories, exposing it to cosmic rays.

Two SLs were equipped with a card carrying eight BTI ASICs. The BTI is a synchronous device and therefore its performance is strictly related to the phase of the clock with respect to the particle crossing time. A 80 MHz FIFO unit [9.17] [9.18] was used to identify the 25 ns time slot assigned to the BTI trigger: the BTI computed parameters corresponding to any time slot were

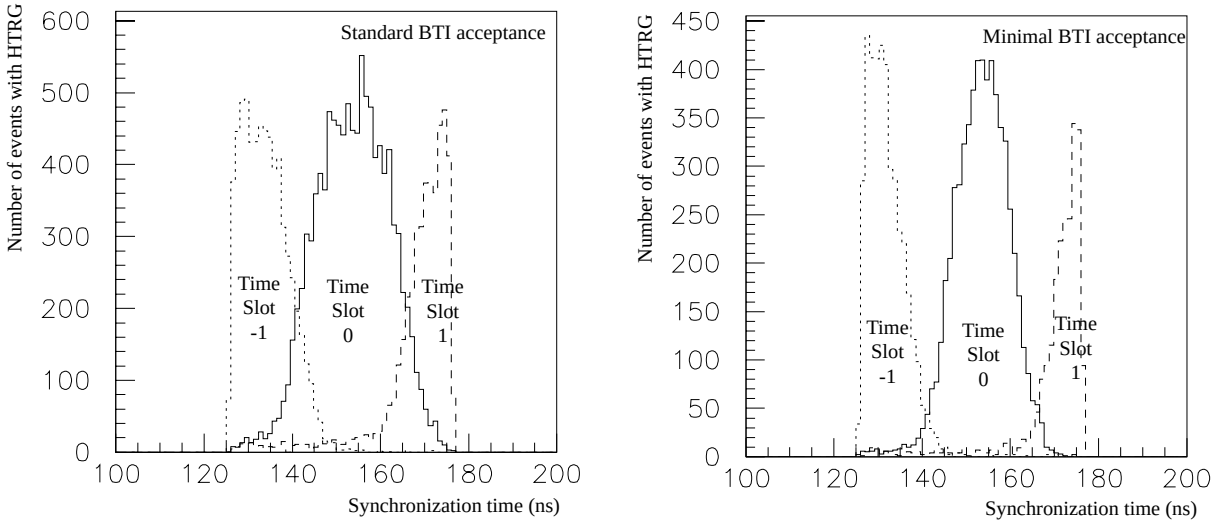


Fig. 9.28: High Quality trigger time slot assignment as a function of the synchronization time.

stored within the FIFO. The BTI data and the drift times were recorded using 960 MHz TDCs with multihit capability [9.20].

The recorded drift times were used to reconstruct beam tracks using a linear least squared fit. Only hits with drift times below 400ns were considered. The space-time conversion was linear using an average drift velocity of 56 μm/ns and all three or four points tracks with a χ^2 fit probability better than 0.1% were selected.

The time difference between the event trigger and the BTI internal clock is computed using a TDC channel with a 50ns jitter. This difference defines the synchronization time of any event and can be used to select the events finding their phase with respect to the BTI clock. The performance of the BTI as a function of the synchronization time is shown in Fig. 9.28 for the HTRG signals in the standard configuration and in the minimum acceptance configuration acting on the alignment tolerance. As expected the dependence of the fraction of HTRGs on the synchronization time is a periodic function.

This dependence is much more important for the minimal acceptance than for the standard acceptance, because of the stricter requirement on alignment of the hits.

We verified that the probability of missing an HTRG in the ±4ns range around the distribution center introduces only a 1% systematic effect in the evaluation of the HTRG fraction.

The analyzed sample satisfies the following criteria:

- 3 or 4 points fitted track choosing the best χ^2 track with Prob(χ^2) > 0.1%
- fitted position falling within acceptance of the installed BTIs
- synchronization time within ±4ns from the central value of the central time slot

Position Studies

The BTI provides a position measurement in a reference frame with the origin on its left side (see Fig. 9.7).

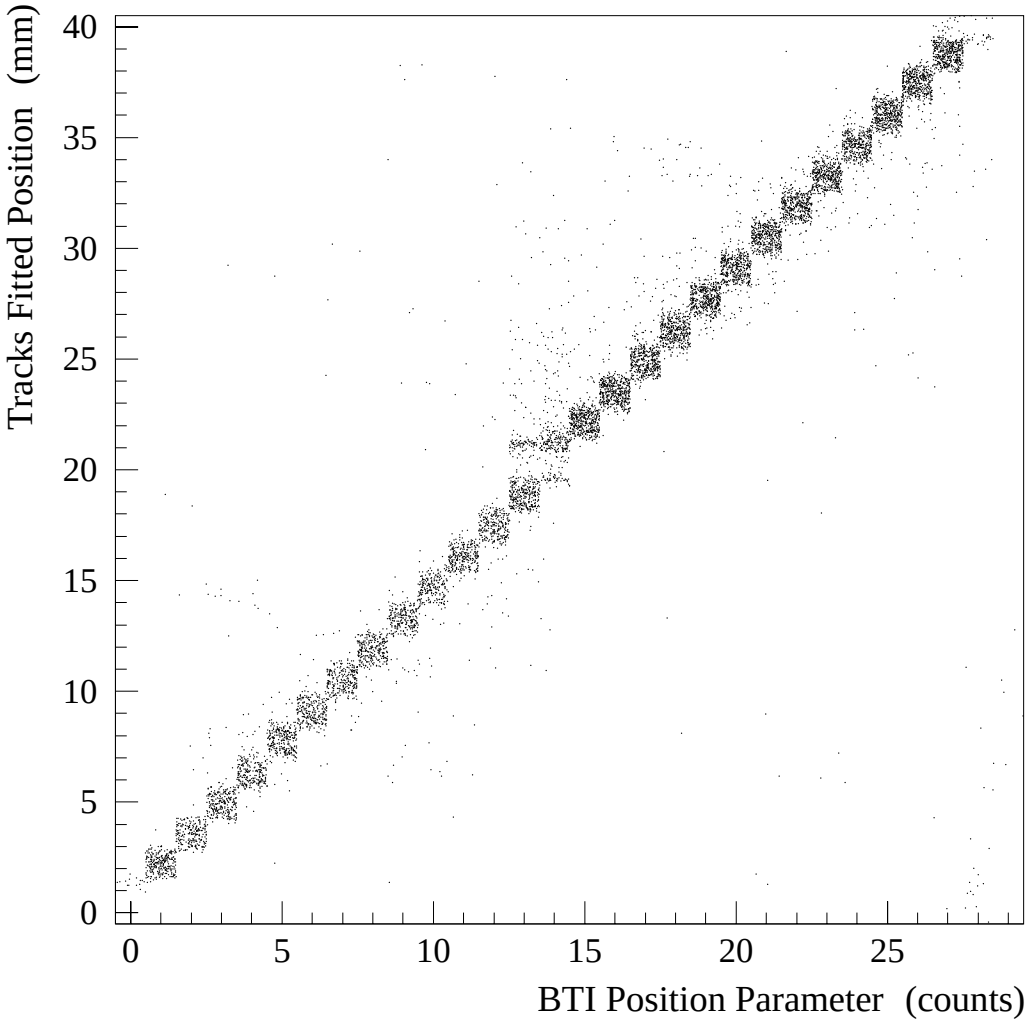


Fig. 9.29: Correlation between BTI position parameter and track fitted position. All triggers in the right time slot were included.

The BTI position can be converted into an absolute position: Fig. 9.29 shows the correlation between the BTI computed position and the fitted track position for triggers issued only in the right time slot.

The difference between the computed position and the fitted position is given in Fig. 9.30: the width of the distribution provides the BTI position resolution.

According to the used BTI configuration, the internal calculations are done using a 0.7mm least count and the trigger is output with a 1.4mm least count. The distribution should therefore have a width $\sigma \sim 1.4/\sqrt{12} \sim 0.4mm$ in the hypothetical case that all the events would fall in one bin.

The found resolution exhibits a slightly larger width, but it well agrees with expectations: HTRGs should have a better resolution than LTRGs, because of the larger lever arm for the calculation.

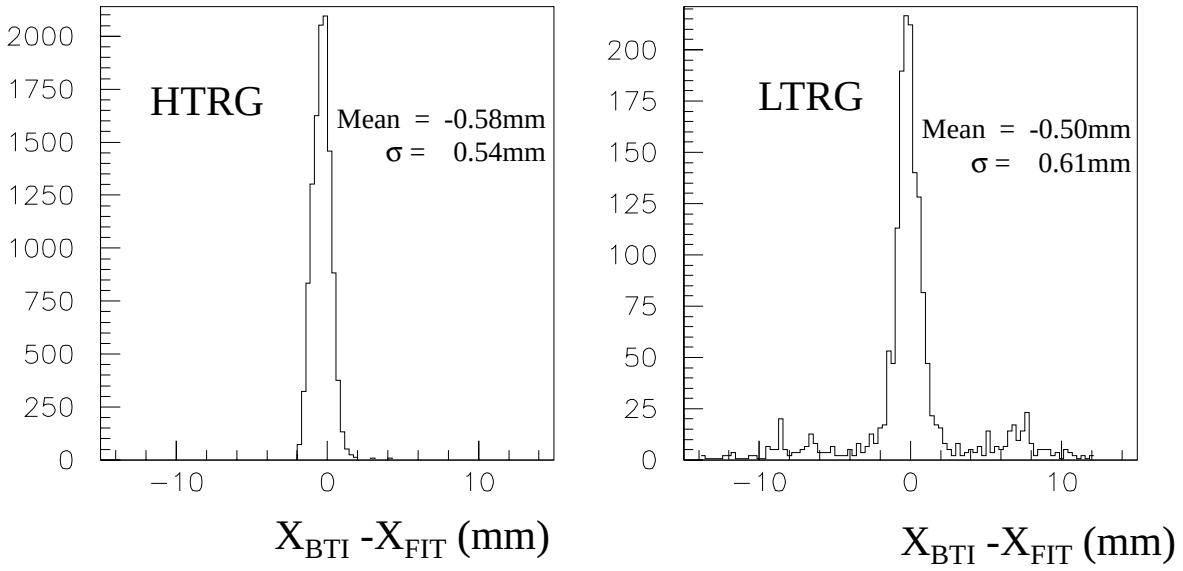


Fig. 9.30: Position resolution for different trigger qualities.

Direction Studies

The performance check of the BTI angular calculations was done using cosmic rays. The BTI is not computing directly the track direction, but it determines a k-parameter related to the angle of incidence. The correlation between the measured k-parameter and the fitted track direction is shown in Fig. 9.31. Although the angle itself is never internally used, for sake of clarity it is better to compare the measured and fitted angle, converting the computed k-parameter into the angle ψ. Their difference is shown in Fig. 9.32, for different trigger qualities.

Once again the result matches expectations($\sigma \sim 60/\sqrt{12} \sim 17 mrad$ ~ 1 degree).

BTI Efficiency

The BTI triggers are assigned to 25 ns time slots. The time slot assignment determines the parent bunch crossing due to the mean-timer principle. If the trigger is found in the expected time slot the bunch crossing is correctly identified, otherwise it is wrongly fixed. Hence the BTI efficiency is defined as the probability per event to have a trigger in the right time slot.

The uniformity of the BTI response along the cell is shown in Fig. 9.33: the BTI efficiency as a function of the particle impact point at normal incidence is flat. This fact implies that the drift cells design has indeed met the basic linearity requirements.

But the space-time linearity relation required to assure a correct performance of the BTI is not achievable in the whole angular range. The BTI is still able to trigger correctly until the deviation from linearity is below 25ns, but at very large angle there are much bigger deviations.

Fig. 9.34 and Fig. 9.35 show respectively the behaviour of the BTI trigger efficiency and the probability of out of time triggers in selected 5° angular intervals, separately for the full sample and the four hits sample.

The BTI response is almost flat up to about an angle of incidence of 30°. Beyond this value the BTI starts to fail in finding alignments of four hits at the right time and simultaneously

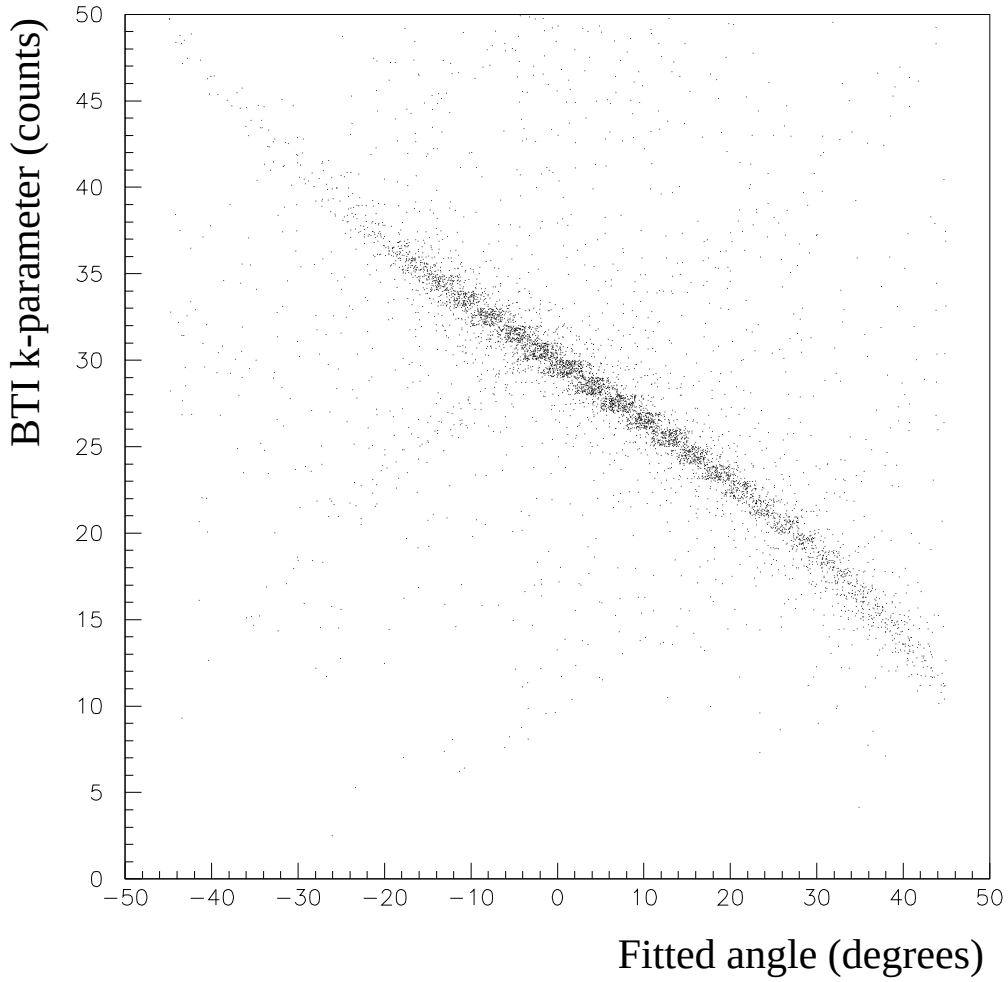


Fig. 9.31: Correlation between the computed k-parameter and the fitted angle. All triggers in the right time slot were included.

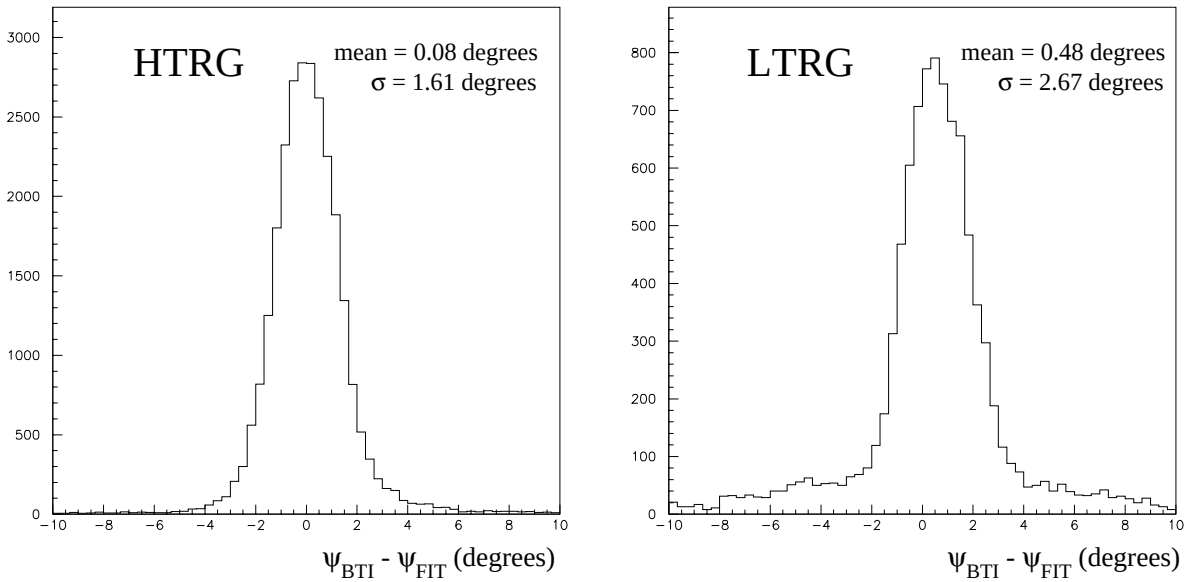


Fig. 9.32: Angular resolution for different trigger qualities.

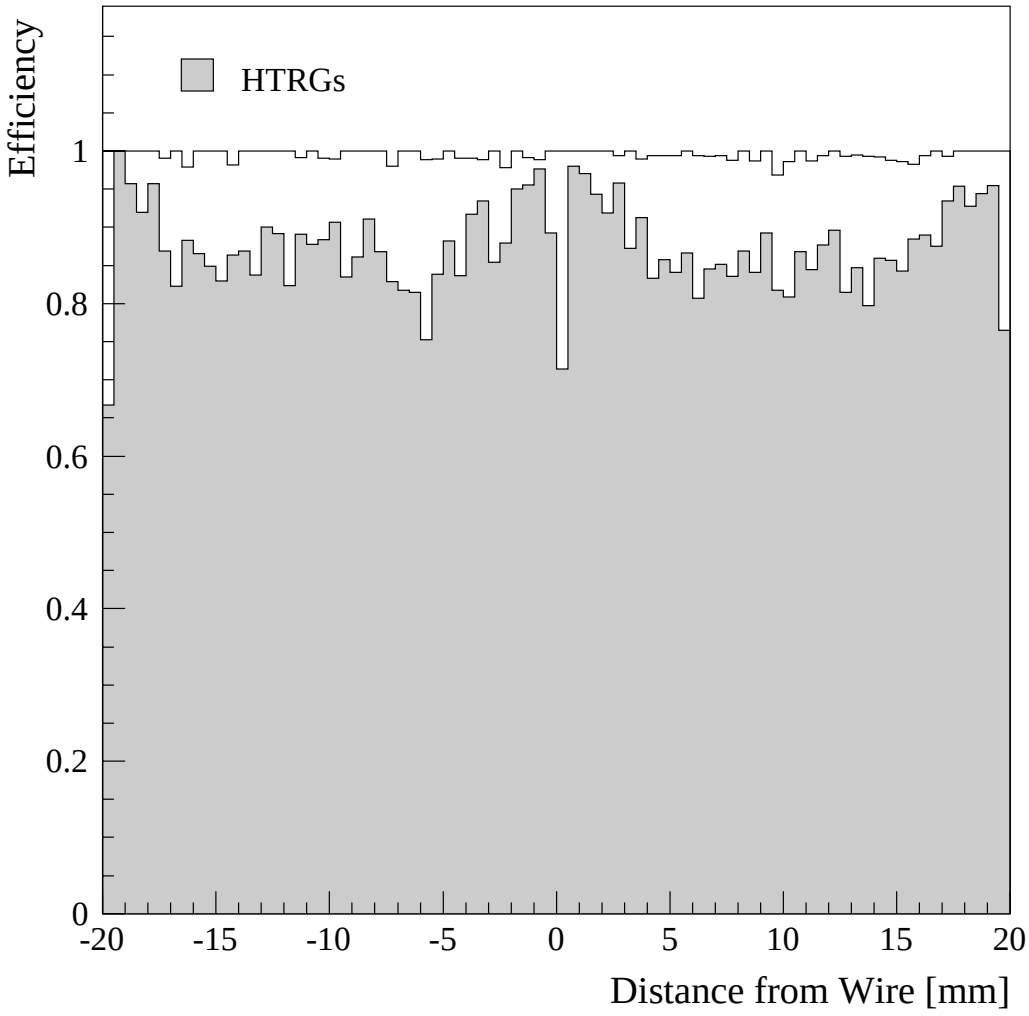


Fig. 9.33: Efficiency of the BTI at normal incidence as a function of the crossing point inside the drift cell.

the probability of finding an out of time HTRG increases. The failure is dramatic for the full sample and rather more limited for the sample of fitted four hits tracks. This fact confirms that the HTRG loss in not due to errors in the BTI design but to the unavoidable linearity degradation of the cell with increasing incidence angle.

The out of time triggers are mostly issued in the time slot just before the right time slot. Therefore activating the LTS mechanism a fraction of the good LTRGs will be canceled. Unfortunately LTRGs will be dominant at very large angle. Anyway it is important to remind that the chamber was the first full size prototype and improvements in its performance should be expected in the final version.

Another interesting check is the efficiency in the different configurations that were used for the BTI. The results for normal incident muons are summarized in Table 9.5. The relative fraction of LTRGs and HTRGs is consistent with the already measured probability of δ-ray generation in the interaction of the muon with matter[4].

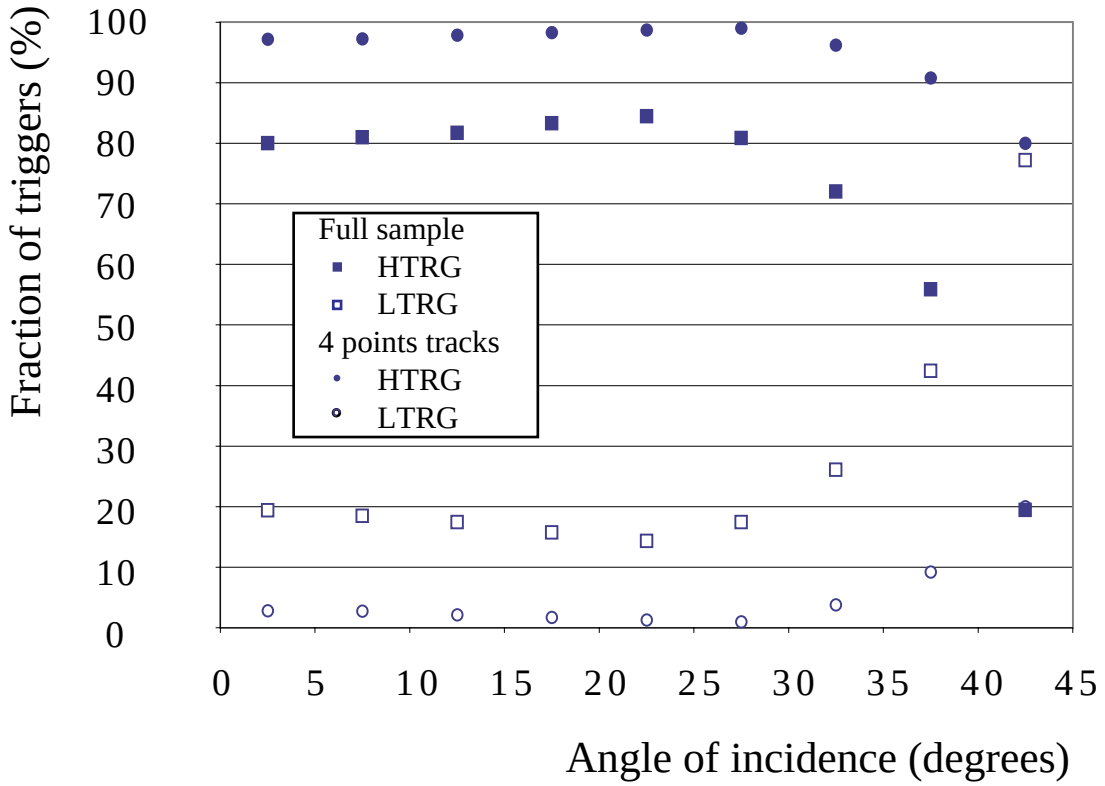


Fig. 9.34: Relative fraction of HTRGs (full symbols) and LTRGs (open symbols) in the BTI as a function of the muon angle of incidence. The circles refer to the subsample of fitted four points tracks, while the squares refer to the full selected sample. The efficiency of the BTI is given by the sum of HTRGs and LTRGs and is 100% everywhere except at normal incidence due to the presence of the walls of the drift tubes.

It is clear that the BTI inefficiency is negligible, but it is also evident that the LTS mechanism, activated for all configurations except the first one, is cutting a small amount of good triggers.

Table 9.5: Efficiency figures for the tested configurations.

BTI acceptance	LTS	HTRG fraction	LTRG fraction	Inefficiency
Standard	off	84.0%	15.6%	0.3%
Standard	on	85.1%	13.6%	1.3%
Minimum	on	70.7%	28.2%	1.1%
Maximum	on	84.8%	13.8%	1.4%

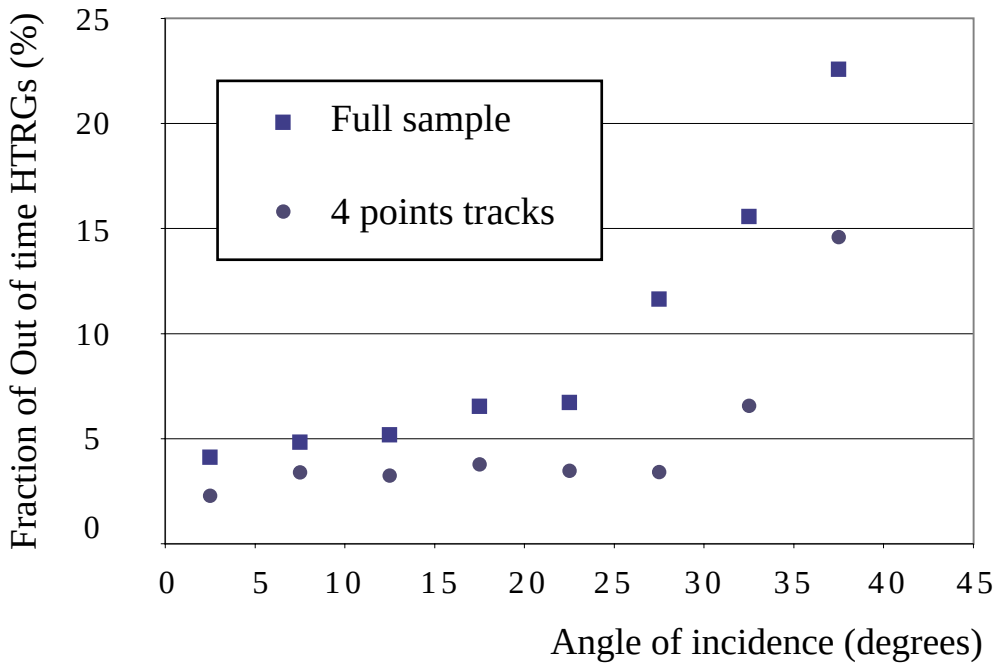


Fig. 9.35: Probability per event of out of time HTRGs in the same BTI at different time slots as a function of the muon angle of incidence.

Summing the HTRG fraction to the LTRG one, the overall trigger rate is roughly constant in all cases. Therefore in the minimal acceptance configuration there is just a different population, with HTRGs becoming LTRGs, rather than the creation of inefficiencies.

The maximal acceptance configuration result shows that the acceptance requirement provided by the standard configuration is sensible, since no real efficiency gain is obtained relaxing the alignment tolerance.

BTI Efficiency in Magnetic Field

Data were taken in magnetic field in several configurations [9.14]. Unfortunately for most of these configurations the BTI prototype data were not available due to system faults, but the drift-times were correctly recorded and therefore the analysis of the trigger performance using the full scale BTI model could be successfully performed. Thus, in this section, we will only quote the results of the software model.

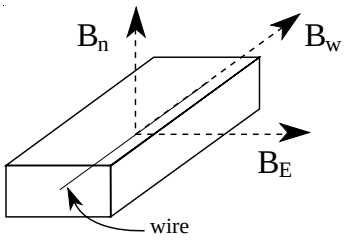


Fig. 9.36: Definition of the magnetic field components.

The magnetic field components are defined in Fig. 9.36 with respect to the chamber layout: B_n is the component perpendicular to the chamber, B_w is the component parallel to the wires and B_E is the component parallel to the electric field.

The global effect of a magnetic field is an elongation of the electron drift path to the anode, resulting in a longer maximum drift time. It also introduces deviations from linearity of the space-time relationship, that are quite important for $B_w \neq 0$.

Data were taken with the chamber normal to the beam for several values of B_n or B_w or B_E separately, keeping null the other field components.

When the chamber was inclined in the magnetic field the situation was more complex: in the case of vertical wires the magnetic field had the two components $B_w = B\sin\psi$ and $B_n = B\cos\psi$, while in the case of horizontal wires the two components were $B_E = B\sin\psi$ and $B_n = B\cos\psi$.

The trigger efficiencies for the situation $B_w \neq 0$, $B_E = B_n = 0$ are shown in Fig. 9.37 for several track inclinations.

The efficiency shows a marked dependence on the field sign for inclined muons. This effect is explained from the drift lines distortion introduced by the magnetic field. The major effect is the tilting of the drift lines by the Lorentz angle in such a way that they do not appear anymore normal to the beam at $\psi = 0°$. Therefore the beam inclination with respect to the drift lines for one

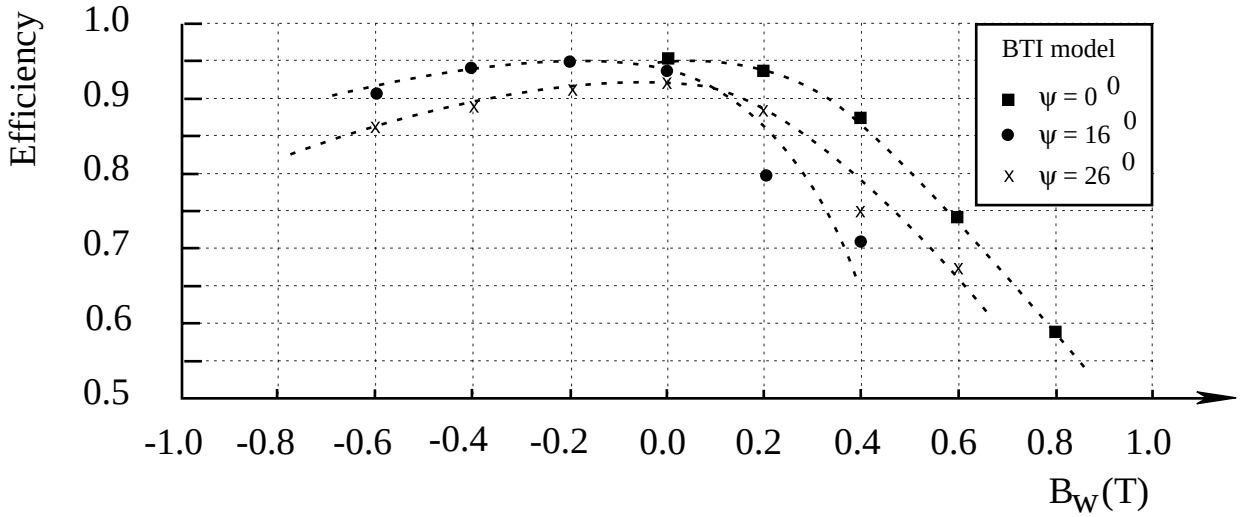


Fig. 9.37: Efficiency of the BTI software model as a function of B_w for several track inclinations. The lines are drawn just to guide the eye.

Table 9.6: Efficiency of BTI model with $B_E \neq 0$ at normal incidence.

B_E(T)	0.0	0.5	1.5
B_n(T)	0.0	0.0	0.0
B_w(T)	0.0	0.0	0.0
Efficiency	0.943	0.936	0.887

Table 9.7: Efficiency of BTI model with $B_n \neq 0$ at normal incidence.

B_E(T)	0.0	0.0	0.0
B_n(T)	0.0	0.5	1.0
B_w(T)	0.0	0.0	0.0
Efficiency	0.943	0.946	0.483

field sign approaches the normal and for the other sign is larger than the chamber nominal inclination. Of course the other sign of the chamber angle with respect to the muon beam direction should cause the symmetric behaviour.

The efficiencies measured for the simple magnetic field configurations are reported in Table 9.6 and Table 9.7, while for the inclined beam situations the data are reported in Ref 1.

In CMS the BTI is expected to work on chambers in which the field will be generally well below 0.2T. Only at some corner chambers the field is expected to be highly inhomogenous with components B_n varying from 0T to 0.8T and B_w or B_E varying from 0T to 0.3T.

Looking at the obtained results we see that the effect is negligible for a field with components $B_n < 0.5$T and B_w or $B_E < 0.2$ T. The CMS region where the magnetic field exceeds these values is only the far corner of the first muon station. Since this region is fully covered by the forward chambers we do not expect any trigger loss.

Performance of the BTI in the θ-view

The θ-view SL is looking at the tracks in the non-bending plane projection. Therefore the muon tracks will be distributed about the line connecting to the production vertex, due to the effect of multiple scattering. Each BTI in this view will see tracks coming from the vertex at fixed angle depending on its geometrical position. The BTIs will therefore be programmed to forward only tracks reconstructed within a predefined angular acceptance. The foreseen standard acceptance is an angle of about 11mrad.

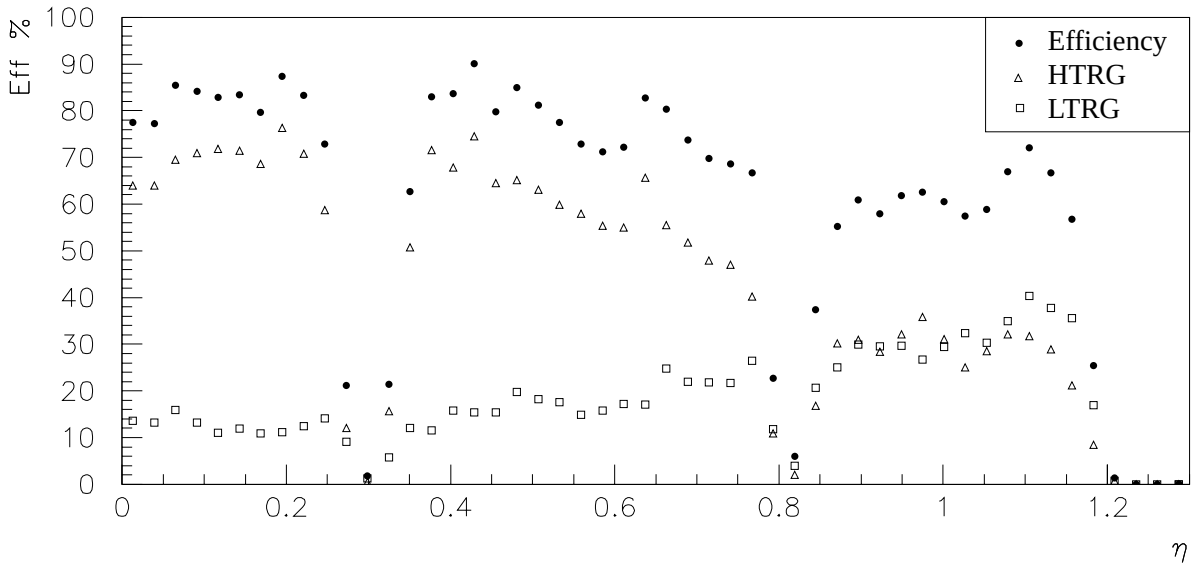


Fig. 9.38: Efficiency of the θ-view trigger as a function of pseudorapidity for a sample of muons of 17GeV/c < p_T < 20 GeV/c

The BTIs close to the forward walls are the ones that will experience the worst situation due to the stray magnetic field: in particular MS1 will be the most suffering station.

All these effects were included in the simulation program and Fig. 9.38 shows the efficiency of the θ-view BTI in MS1. The effect of the linearity degradation with large angle combined with the magnetic field distortion is evident. A reasonable global efficiency is anyway reached, although at the far end the fraction of HTRGs is quite poor.

9.10.2 Track Correlator and Trigger Server

The TRACO and TS devices are interacting at several stages making selections on track quality and basing the choice on both devices sorting mechanism. In particular the TRACO is using ghost suppression algorithms based on TSθ results.

It is quite difficult to isolate contributions of the single device without having at least a small contribution on the effective flow chosen on the other one. The simulation results [9.6] are therefore presented at the TS output for particular settings of both devices and must be considered as global results, unless explicitly specified.

However we must remind that TRACO and TS have very different impact on the quoted performance: while the contributions on single muon efficiency and noise are to be considered more or less equally divided, resolution and acceptance cuts are mainly connected to the TRACO algorithms and dimuons efficiency is more related to TS design.

Efficiency

The efficiency of the TRACO-TS system to find a track candidate when a single muon track traverses the detector, was studied using two samples:

– the first sample consisted of 10000 single muons of p_T = 100 GeV/c, generated inside the iron in front of one correlator with incident angle -60° ≤ ψ ≤60°

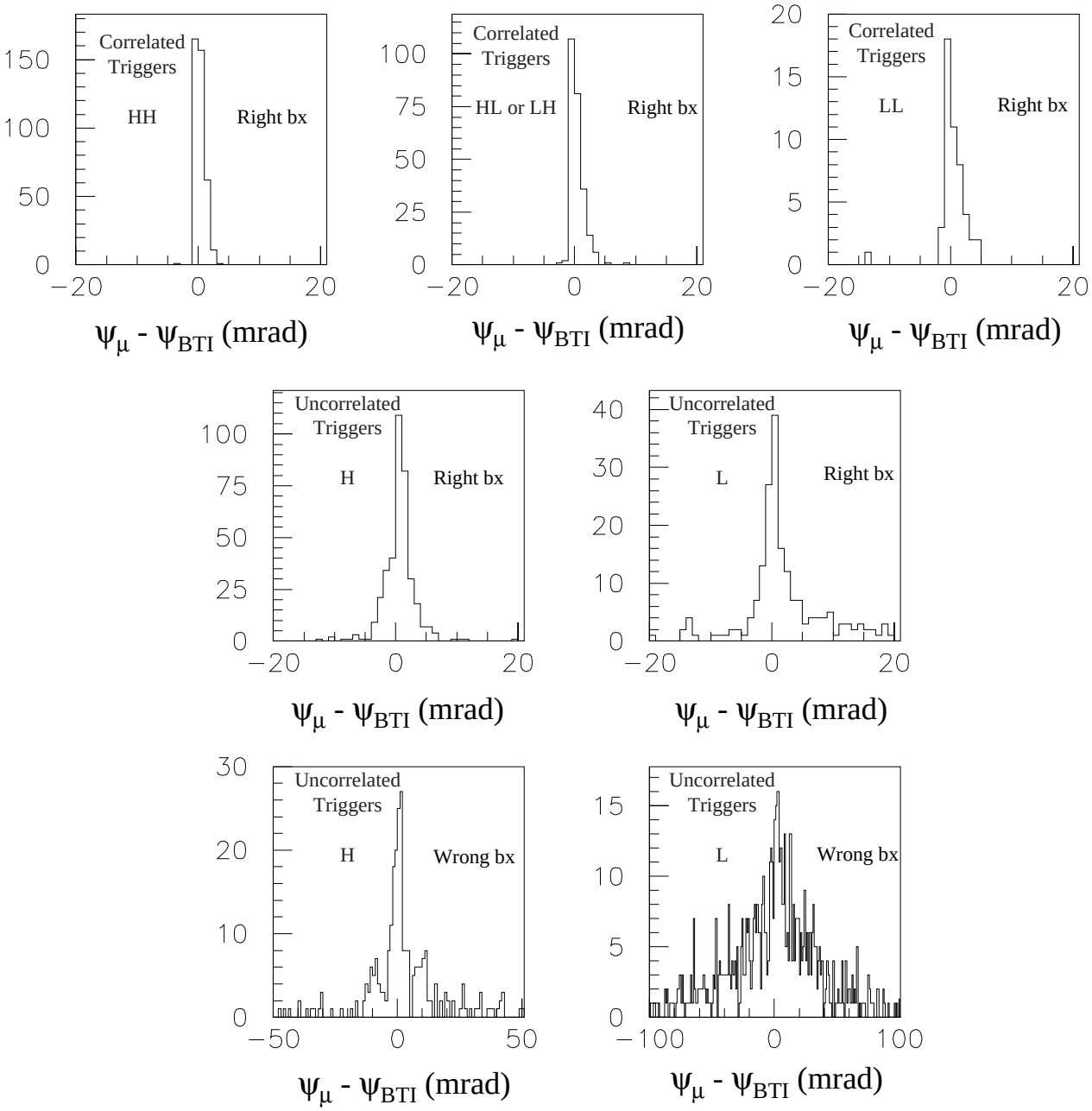


Fig. 9.39: Difference between the generated and the computed angle for different quality of the triggers. Notice the different scale for the histograms at right bx and the histograms at wrong bx.

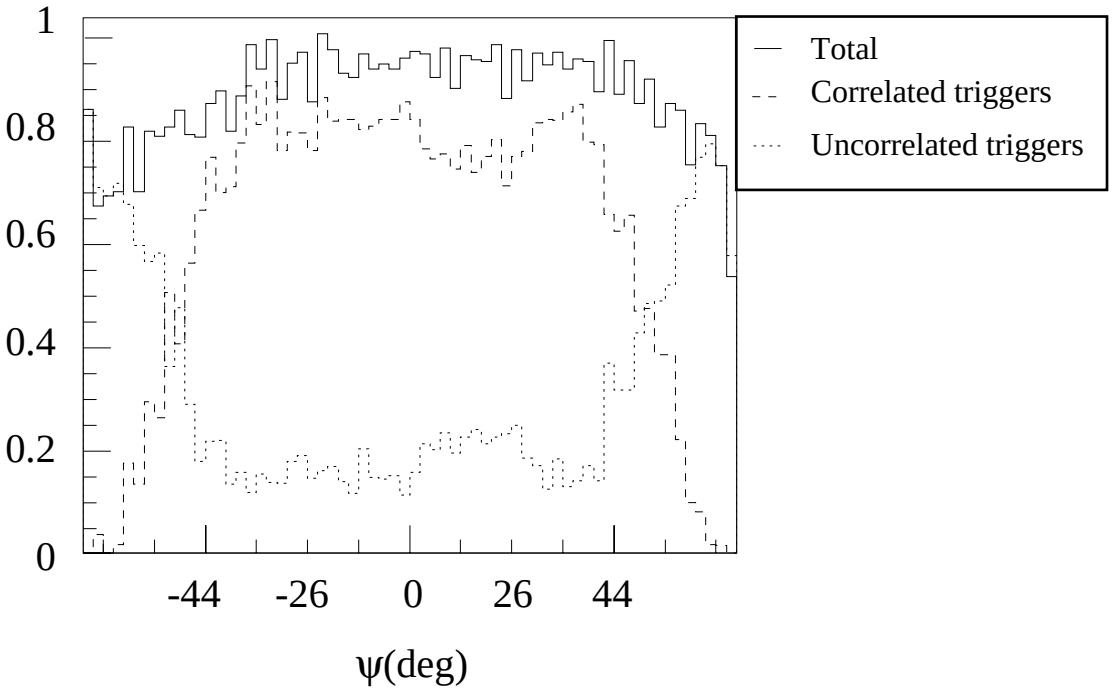


Fig. 9.40: TRACO efficiency as a function of the incident angle (Notice that the scale is not linear).

– the second sample consisted of 100000 single muons generated from the interaction vertex with 3.5 Gev/c ≤ p_T ≤ 300 Gev/c.

Fig. 9.39 shows the difference between the computed incidence angle and the actual incidence angle of the muon for different track quality and, only for the uncorrelated triggers, for cases where the determined bunch crossing is the correct or the wrong one.

It is evident from the distribution that the resolution of uncorrelated triggers is worse than the one of correlated triggers. Besides the angle calculated for the uncorrelated LTRGs misidentifying bunch crossing has got a wide range.

Fig. 9.40 shows the efficiency of the TRACO as a function of the angle of incidence: the TRACO has a flat probability (~80%) to correlate within its 45° acceptance range, while outside this range only uncorrelated triggers are available. We do not expect anyway to trigger on tracks with angle larger than 45°.

The performance as a function of the muon momentum was evaluated at the Trigger Server output for three relevant major configurations of the TRACO acting on the uncorrelated LTRGs acceptance:

This configurations were:

– *L accepted on any θ trigger*: uncorrelated LTRGs are accepted only if they areconfirmed by a BTI trigger of any quality in the θ view. This is supposed to be the standard configuration for data taking

– *L accepted on HTRGθ trigger*: uncorrelated LTRGs are accepted only if they are confirmed by a BTI trigger of HTRG quality in the θ view

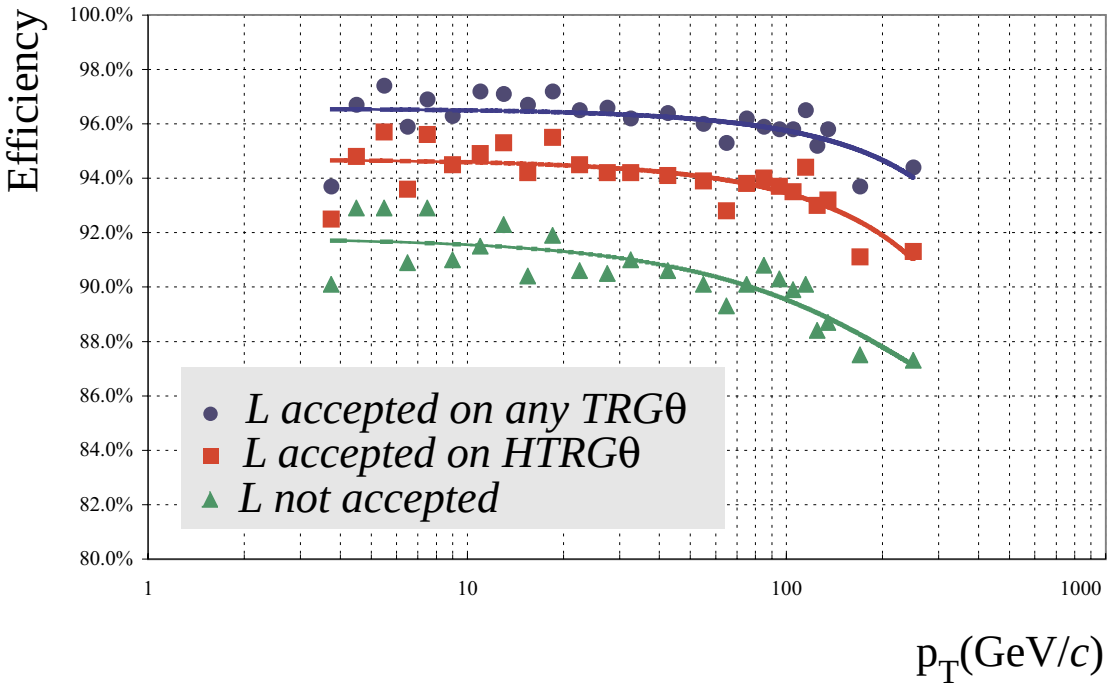


Fig. 9.41: Local drift tubes trigger efficiency as a function of transverse momentum for the major configurations.

– *L not accepted*: uncorrelated LTRGs are not accepted

The performance for the four muons station, once corrected for station acceptance is the same: therefore we will give only results for station 1.

Fig. 9.41 shows the efficiency, corrected for the muon chambers geometrical acceptance, for the three selected conditions. Before activating the complete suppression of uncorrelated LTRGs there is clearly space for an intermediate step that causes a negligible efficiency loss. But even in the case we are forced to reject uncorrelated LTRGs, the efficiency remains in a sensible range.

In the standard configuration the fraction of events giving triggers only at the correct bunch crossing is slowly decreasing from ~66% at 5 GeV/c to ~60% at 300 GeV/c, while events not triggering at the right bunch crossing are in fact giving triggers only at wrong bunch crossings.

The relative fraction of triggers at the correct bunch crossing divided by track quality is shown in Fig. 9.42 in the standard configuration, showing a roughly constant value.

Since the sample consisted of single muons, the noise markers are the fraction of two tracks per event selected by the TRACO and the quantity of out of time triggers.

Fig. 9.43 reports the fraction of Second Tracks generated after applying the standard TRACO/TS selection mechanisms and Fig. 9.44 shows the average fraction per generated event of out of time triggers.

Therefore the uncorrelated LTRG suppression, despite generating a large inefficiency, has a limited impact on the noise reduction.

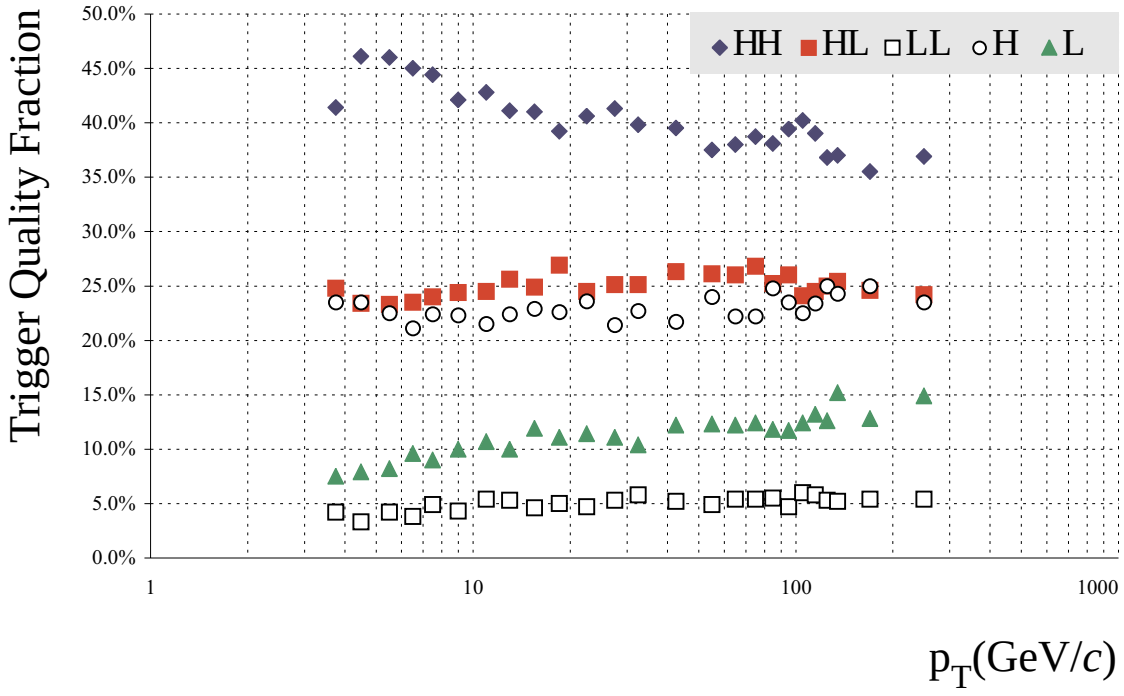


Fig. 9.42: Relative fraction of triggers divided by quality as function of transverse momentum

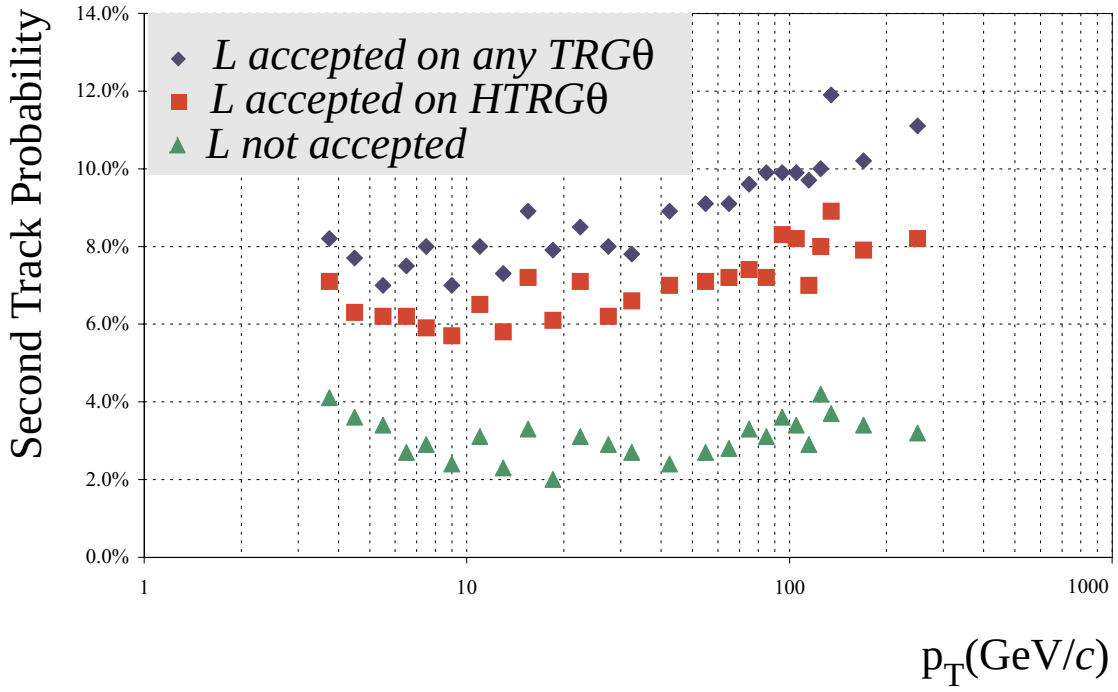


Fig. 9.43: Fraction of Second Tracks per events as function of transverse momentum for the major configurations

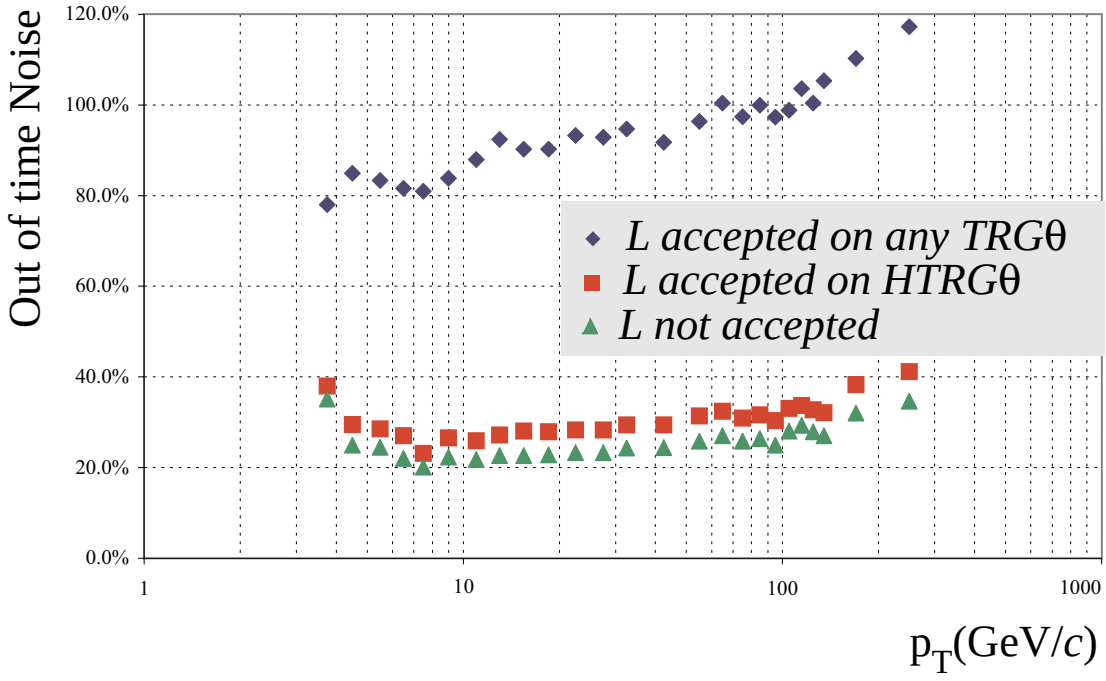


Fig. 9.44: Fraction of out of time triggers as a function of transverse momentum for the major configurations

Since the θ-view BTI efficiency is decreasing with pseudorapidity we could expect effects on the performance of the local trigger. The θ-view filter is anyway acting only on uncorrelated LTRGs and the impact is quite low, as can be deduced from Fig. 9.45.

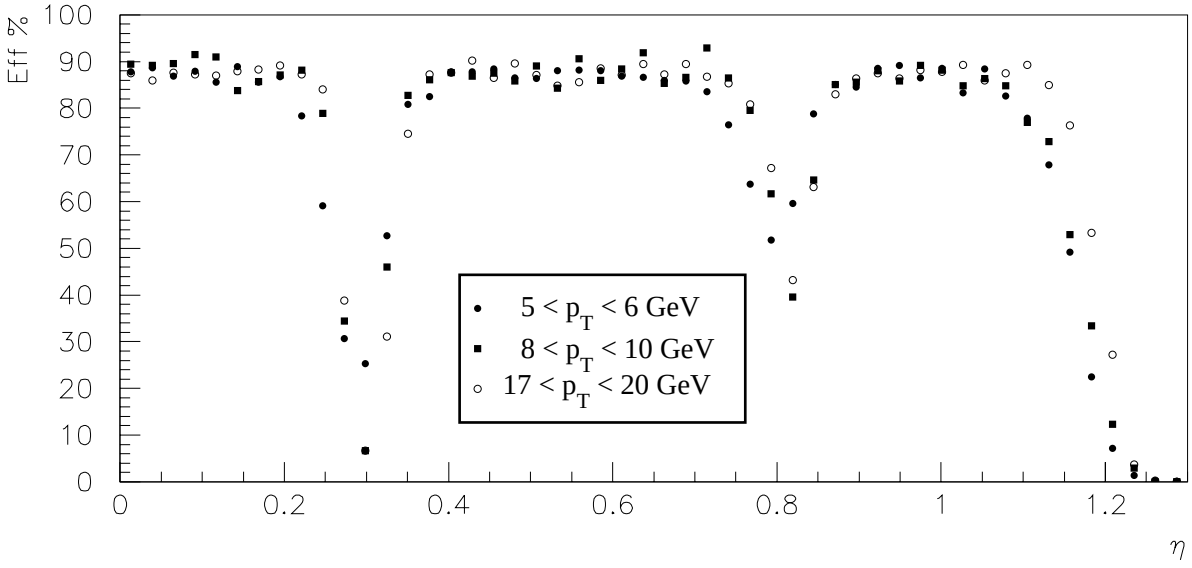


Fig. 9.45: Efficiency of the drift tubes local trigger as a function of pseudorapidity.

9.11 Noise Reduction

The design of the trigger devices was done with the purpose of providing a robust and efficient system. Unfortunately the way to meet these requirements introduces a certain number of redundancies in the system causing an important fraction of false or duplicated triggers [9.3] [9.6].

9.11.1 Noise Generation Mechanisms

The BTI trigger algorithm can actually work requiring only three layers of staggered tubes. The drawback to three layers algorithm is the fact that an inefficiency or a bad measurement on any of the cells becomes an inefficiency or a wrong trigger. The introduction of the fourth layer with the minimal request of an alignment of three out of four hits maximizes the efficiency and minimizes the wrong measurements. But some spurious alignments of three hits can occur at any bunch crossing, depending on the actual track crossing position and in direction.

Most of the bad alignments are generated from the unavoidable left-right ambiguity even at several bunch crossing distance from the alignment of the four hits.

An example of the mechanism is shown in Fig. 9.46: a real track orthogonal to the chamber is displayed and the hit positions are marked with small circles on the track line. The BTI, looking for alignments of at least three hits, is able to find the alignment corresponding to the real

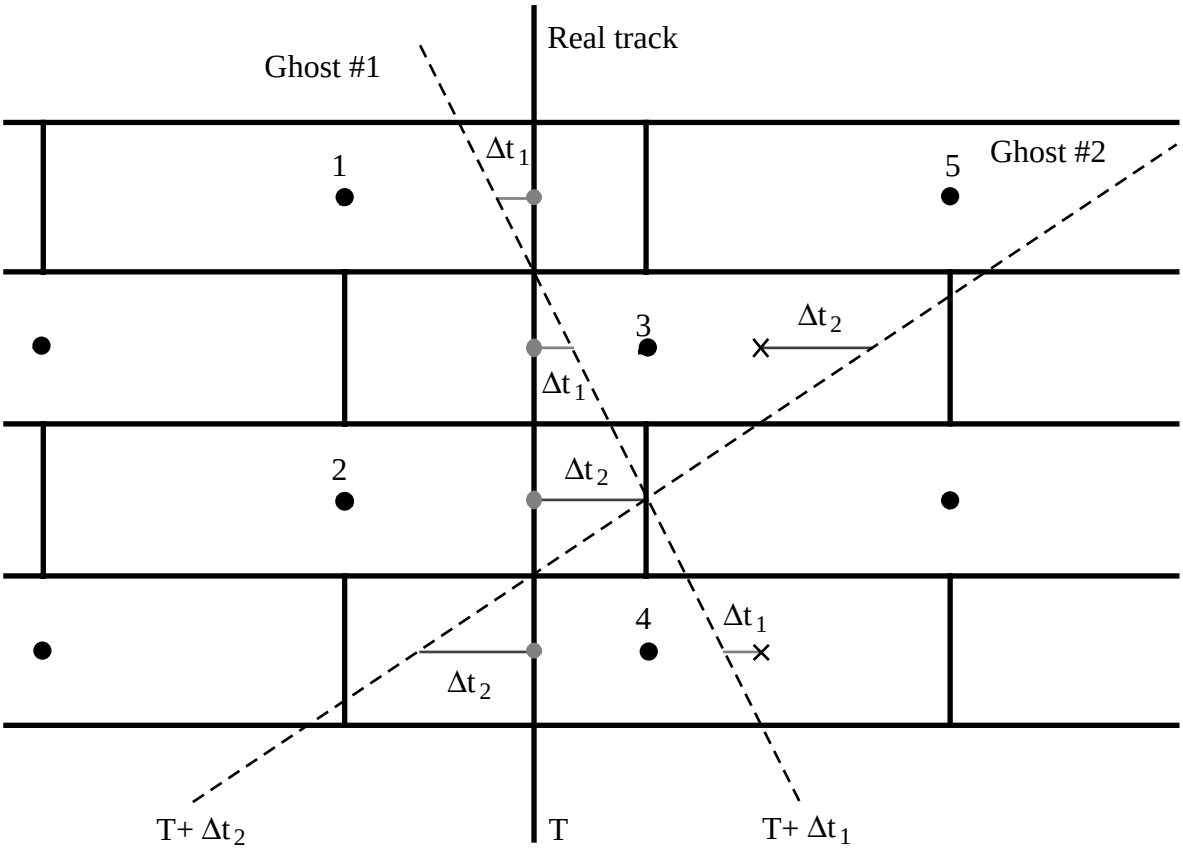


Fig. 9.46: Illustration of the ghost generation mechanism inside BTI.

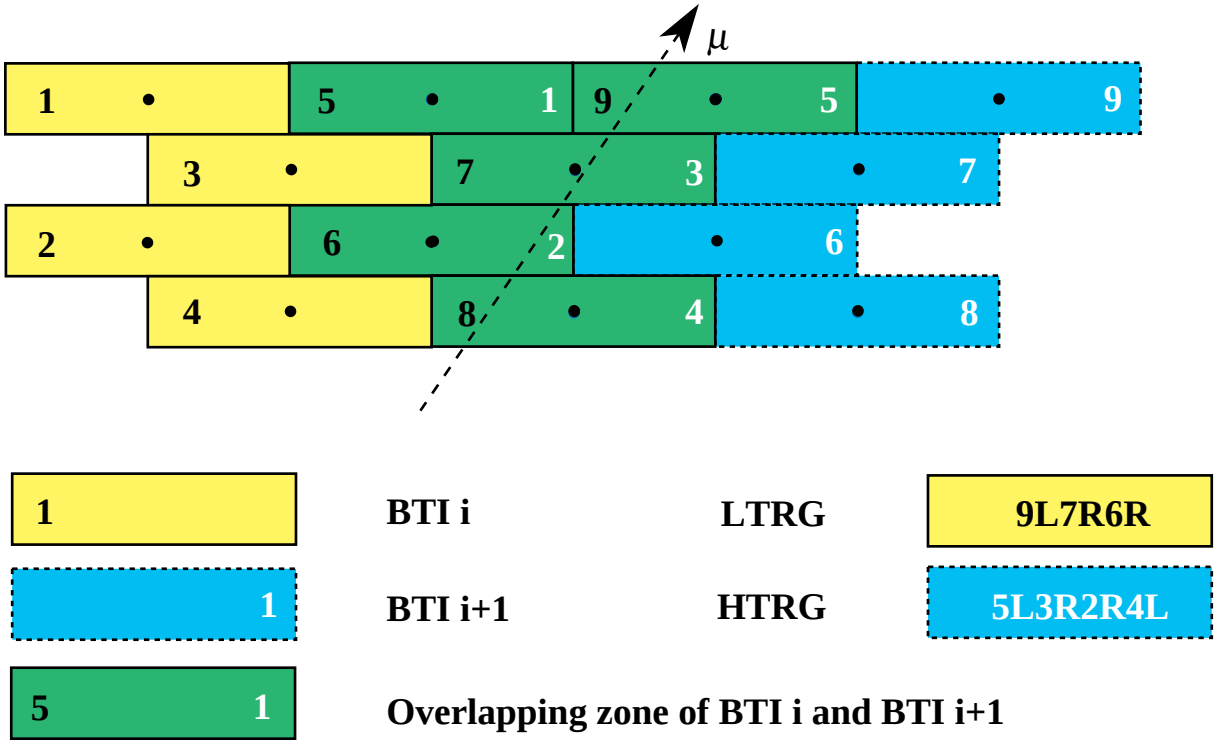


Fig. 9.47: Illustration of the irreducible redundancies between overlapped BTIs.

track, but other two tracks are detected. These tracks, called ghost tracks, correspond to alignments of a mixture of real hits and their mirror images. Indeed the BTI supposing that wire 2 is inefficient and supposing that the signal of wire 4 comes from the right side of the tube, finds a false alignment at time Δt_1 after the right bunch crossing. In the same way, supposing that wire 5 is inefficient, the BTI finds another ghost track, formed from the signals of wires 2 and 4 and the mirror image of signal from wire 3, at time Δt_2 before the right bunch crossing.

This effect occurs inside the BTI at different bunch crossings and therefore generates temporal noise: let's call the ghosts generated by this mechanism *noise of type I*.

Furthermore in order to be fully efficient the trigger system provides some overlapping between adjacent devices: one BTI is overlapped by five cells to its neighbours and BTIs in the outer Superlayer are always assigned to three consecutive TRACOs.

The overlap between BTIs is foreseen in order to minimize the impact of the loss of one device on the trigger efficiency, since the remaining one can be programmed to partially cover the dead area switching on some redundant patterns.

It is not possible to define a set of completely non-redundant patterns and therefore some of them are available in two consecutive BTIs: in fact there are five redundant patterns generating LTRGs on the devices close to the one generating the HTRG at the same bunch crossing.

In Fig. 9.47 we see a case where a valid HTRG pattern in one BTI is also seen as a valid LTRG pattern in the adjacent one.

Therefore the TRACO will have the chance to make a choice between candidate tracks in adjacent BTIs that are images of the same track, carrying exactly the same information. This is not

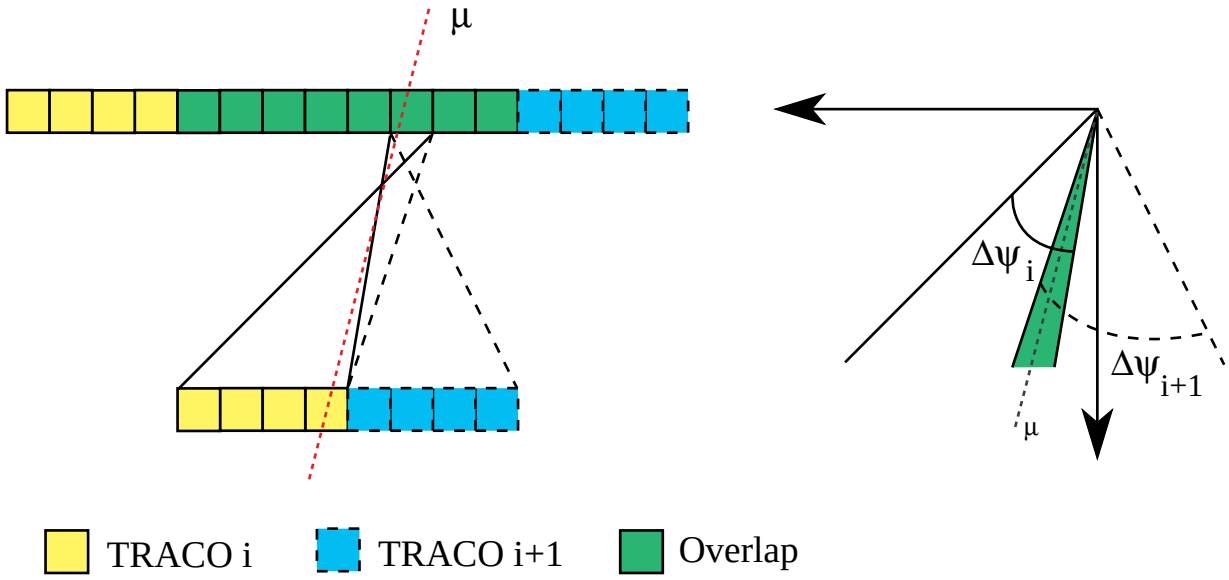


Fig. 9.48: Illustration of the double track selection due to overlapped TRACOs. The solid lines are the acceptance window of the i-th TRACO an the dashed lines are the acceptance window of the (i+1)-th TRACO. The diagram on the right draws the acceptance windows on the same origin to evidence their intersection (shaded region). A muon falling in this intersection region is assigned to both TRACOs

a problem for the First Track sorting, since both are equivalent, but it may result that the TRACO is forwarding the same track twice, with a chance of losing other available candidates. This is a duplication of the trigger at the same bunch crossing and generates spatial false triggers called *noise of type II*.

There is another situation (*noise of type III*) that is generating spatial noise candidate tracks. The BTIs in the outer sorter are assigned to three consecutive TRACOs, being in the left, the central or the right group of the outer SL. The BTI data are sent to each TRACO through a dedicated port. Each port is programmed with a different angular acceptance window, depending on the fact that is communicating to the left, central or right group. These tolerance windows are partially superposing: therefore a candidate track falling in the intersection zone, is forwarded from the BTI to more than one TRACO as shown in Fig. 9.48. Hence, as in the case of adjacent BTIs, adjacent TRACOs can forward to the Trigger Server twice the same track. Again this fact may introduce a bias in the Second Track selection at the TS level.

9.11.2 Noise Reduction Methods

We have seen that there is a temporal noise, due to left-right ambiguity (*type I*), that generates ghost tracks at wrong bunch crossings and spatial noise caused either by redundancy of the BTI equations (*type II*) or by the overlap of the BTI acceptance ports (*type III*), generating copies of the same track.

Some filters have been provided to reduce the overall importance of these effects.

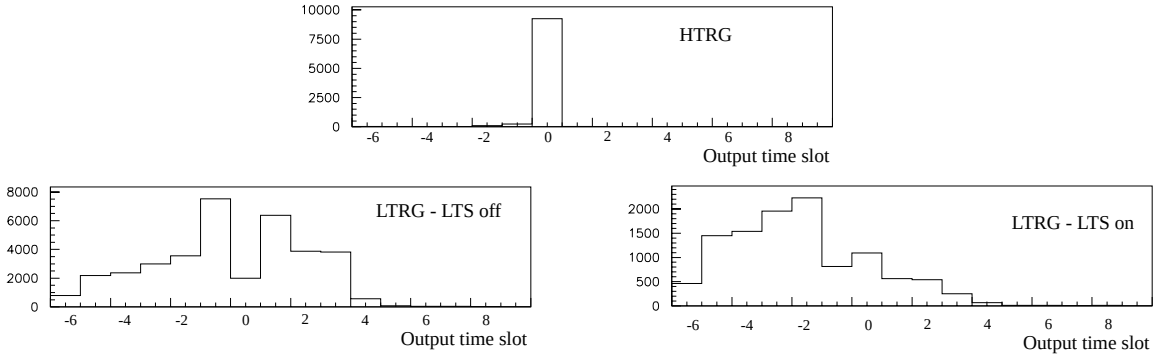


Fig. 9.49: Time distribution of BTI output triggers, for different trigger qualities and configurations.

The BTI can only act on temporal noise. The mechanism provided to perform this task is the Low Trigger Suppression algorithm: the LTRGs occurring in the range (-1 bx,+8bx) around a HTRGs are canceled.

Fig. 9.49 shows the time distribution of BTI triggers for HTRGs and LTRGs without filtering and for LTRGs, once the Low Trigger Suppression is activated.

There is a low probability to issue an HTRG at the wrong time slot, while there is a large number of wrong LTRGs. The average fraction of wrong triggers per event in the different configurations is given in Table 9.8. The noise reduction caused by the LTS mechanism is evident.

Most of the wrong HTRGs are due to noise hits: one of the drift times is different than expected and the alignment occurs around the right angle and position, but at a wrong time, and only a LTRG is issued at the right time. This effect is causing a small efficiency drop when the LTS mechanism is activated, since the right LTRG is cancelled by the nearby wrong HTRG.

The TRACO and TS devices are instead sensitive to all kinds of noise triggers.

Fig. 9.50 shows the time distribution of the triggers after TS processing in the standard configuration, separately for each trigger quality. Correlated triggers containing at least one HTRG segment are quite clean and single uncorrelated HTRGs are reasonably clean. The bunch crossing identification is instead bad for correlated LL and single uncorrelated LTRGs.

Table 9.8: Average fraction of out of time triggers in the BTI at normal incidence.

BTI acceptance	LTS	%H out of time	%L out of time
Standard	off	3.0%	351.2%
Standard	on	3.1%	148.2%
Minimum	on	1.1%	175.6%
Maximum	on	4.1%	165.3%

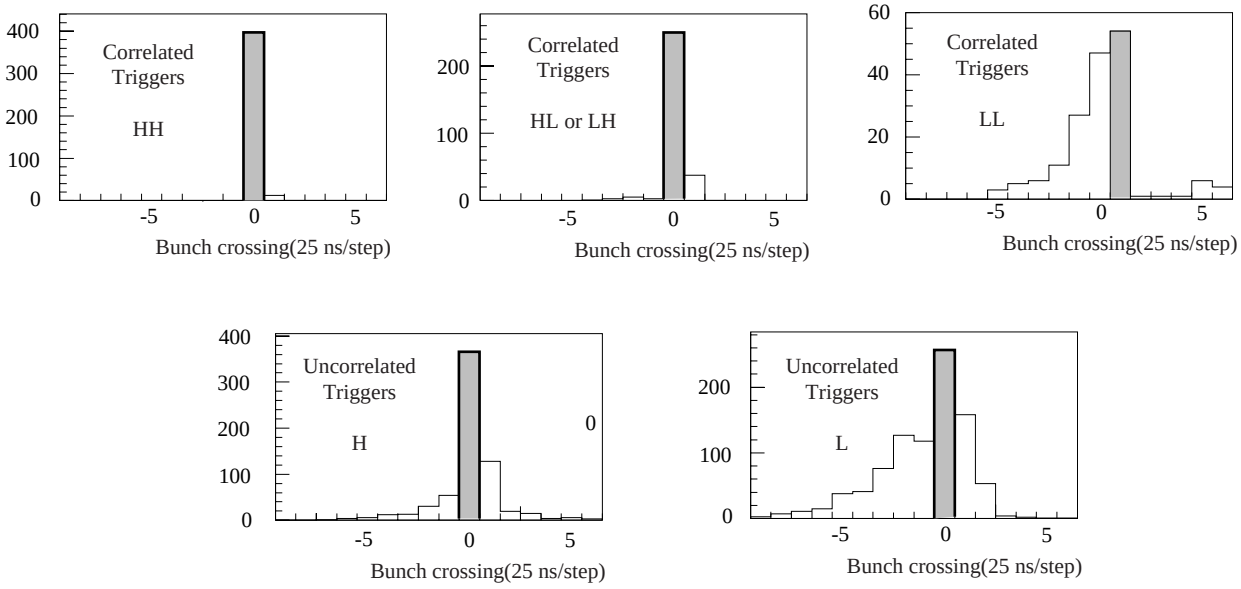


Fig. 9.50: Time distribution of TRACO triggers, divided by trigger quality.

Clearly some noise filtering must be provided to reduce this kind of triggers to an acceptable level. Some of the implemented filters are optional, since the importance of the reduction will only be clear on the field.

In order to reduce the *type I noise* we introduced a LTS mechanism inside the TRACO: the low quality tracks (LL,L_o,L_i) are canceled if a HTRG occurred within the neighbouring bunch crossings. It is possible to suppress triggers at bx from -1 to -4 with respect to any HTRG without any latency addition.

Noise of type II and III can affect only the Second Track selection. It is possible to avoid sending twice the same track using a geometrical suppression filter. If a HTRG was selected in the First Track sorting operation, all the LTRGs in the neighbouring BTIs are removed from the Second Track sorting list. This filter, always active, acts on *type II noise*. A similar procedure, inhibiting Second Track L_o selection, can be applied to neighbouring TRACOs inside to chamber Trigger Server to remove *type III noise*.

The effect of the application of the filters for *type I and II noise* is shown in Table 9.9, compared to a sample of muons at 100 GeV/c in the standard TRACO configuration: the LTS acts on out of time triggers, while the LTRGs suppression on adjacent BTIs acts on the two tracks fraction.

Table 9.9: Effect of type I and type II noise filters. The type III filter is always active.

	Standard	Type I filter on	Type II filter off
Two tracks fraction	6.5%	-	19.4%
Out of time uncorrelated L fraction	53.5%	38.7%	-

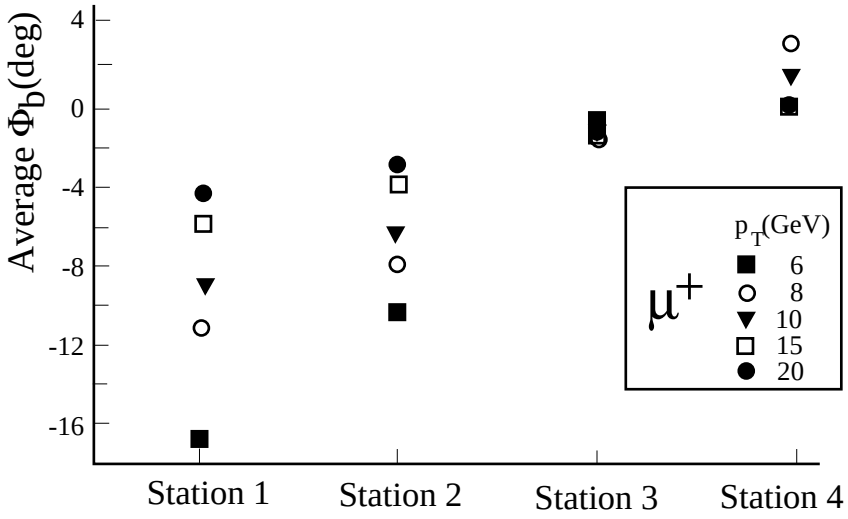


Fig. 9.51: Average bending angle at the different muon measurement stations for some low transverse momentum muons

There is another possible cut to be applied to clean the TRACO output: a programmable tolerance window is implemented for the bending angle. The bending angle for some low momentum muons at all the measurement stations is shown in Fig. 9.51. Indeed there is a large spread for the average bending angle values at stations 1 and 2, while the bending angle is close to zero at station 3 and 4.

We cannot safely apply any cut in the first and second station, while a tolerance on the bending angle can be used for station 3 and/or 4.

Table 9.10 shows the effect of the bending angle cut on efficiency and noise (i.e. the fraction of out of time triggers) for p_T = 8 GeV/c muon tracks. The cut is an 8 bits value to be downloaded to the TRACO.

Table 9.10: Efficiency and noise for different bending angle acceptance windows in the outer stations.

	Station 3		Station 4	
Φ_b cut (degrees	Efficiency (%)	Noise (%)	Efficiency (%)	Noise (%)
51.6	98.0	98.0	98.0	92.6
43.5	97.3	78.0	97.2	75.0
32.3	96.7	65.0	96.8	65.0
17.5	96.4	48.9	95.1	50.7
9.0	94.7	34.2	76.2	30.3

9.11.3 Dimuons Detection Efficiency.

The noise filter algorithms described above were developed to reduce the rate of double tracks at the output of the drift-tube local trigger for single incident tracks, and therefore they only slightly affect the single muon trigger efficiency. On the other hand, the noise suppression is expected to have a larger impact on the efficiency to correctly detect muon pairs when both muons cross the same station, since at most two track segments are delivered at the output of the TS system.

Ideally the trigger system should maximize the efficiency to detect muon pairs and the purity altogether, i.e. the two output track segments should correspond to the two different muons.

The performance of the system on dimuons was studied at the output of the TS with the default algorithm (i.e. with *type I, II and III noise filter on*), for muon pairs crossing a single muon station. Fig. 9.52(a) shows the efficiency of the TS to deliver two track segments in a muon station at the correct bx, when two 100 GeV muons crossed the station, as a function of the distance between the two muons. The small drop in efficiency occurs when the two tracks are closer than the distance of two physical TRACO units, and is due to the noise suppression algorithms, which in this case can reject good track candidates.

In Fig. 9.52(b) the probability of correct identification of both muons by the TS system is shown as a function of their distance. The purity is maximal when the two tracks are separated more than two physical TRACO units. The drop of the probability of correct identification at small track separation is due to the noise, since a ghost track can be selected as the second track candidate.

9.12 Radiation Tests

Since the barrel muon chambers are shielded by the iron yoke against the effects of charged low energy particles, the background flux will be dominated by neutrons produced all around inside the cavern by interactions of the beam halo with the devices on the LHC beam line and the detector itself, that thermalize interacting with the cavern.

Extensive simulation studies [9.21] were done to estimate the rate of background particles at all positions inside CMS. The results of the simulation are shown in Fig. 9.53, where we immediately see that the flux is quite low at the barrel muon chambers positions as compared to the other detectors. The energy spectra of neutrons and gammas were determined. The γ-ray background is about the same in all the stations, while the neutron background is linearly decreasing with energy and is naturally ending around 100 MeV in the outermost station and at few hundred MeV in the innermost one, that is suffering from high energy neutrons flooding through the CMS calorimeters and coil.

Preliminary tests were performed to find the effects of this backgrounds on the performance of the local drift tubes trigger.

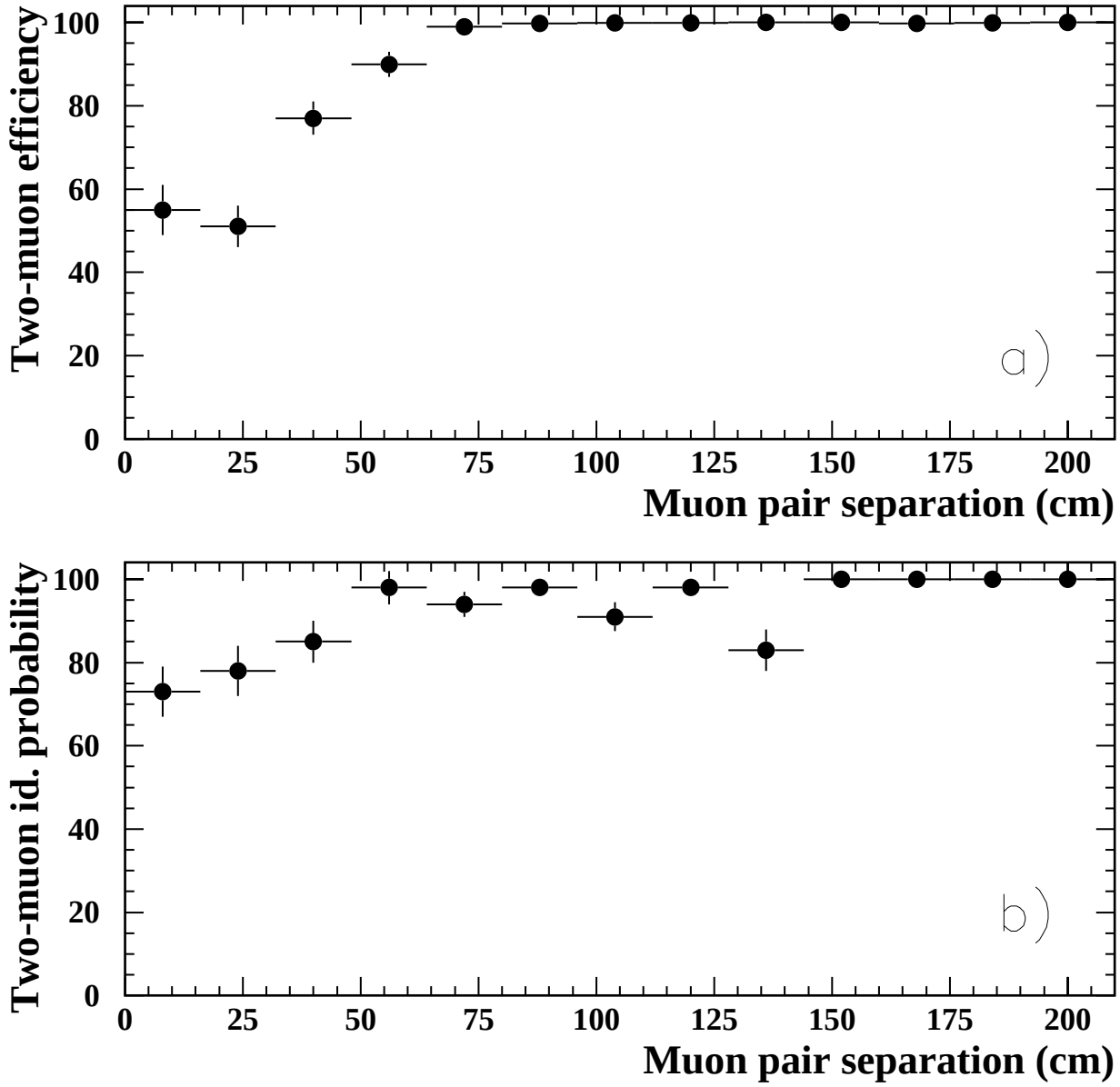


Fig. 9.52: (a) Efficiency of the TS to deliver two track segments in a muon station at the correct bx, when two 100 GeV muons crossed the station, as a function of the distance between the two muons. (b) Probability of the correct identification of both muons by the TS system, as a function of their distance.

9.12.1 Gamma Irradiation Studies

The high rate gamma background is generating noisy hits inside the chamber, disturbing the correct muon track measurement. The full size DTbx chamber prototype, equipped with BTIs, was installed in the CERN GIF test area where a 15 Ci ^{137}Cs radiating 66 MeV source is installed. It was therefore possible to test the performance of the BTI in a radiation environment [9.15]. Data were taken using several filters in front of the source reaching a single hit rate of 10 Hz/cm^2 on the chamber: this rate is the maximum expected rate at LHC in the barrel muon detector due to radiation background.

Table 9.11: Comparison at normal incidence between performance without radiation and maximum radiation.

	%HTRG	%LTRG	Inefficiency	%H out of time	%L out of time
No Radiation	84.0%	15.6%	0.3%	3.0%	351.2%
Radiation 10 Hz/cm^2	83.0%	16.6%	0.5%	2.5%	800.0%

The data were compared to those without radiation looking for differences in the efficiency, the noise probability and the position resolution. Results for efficiency and noise are collected in Table 9.11.

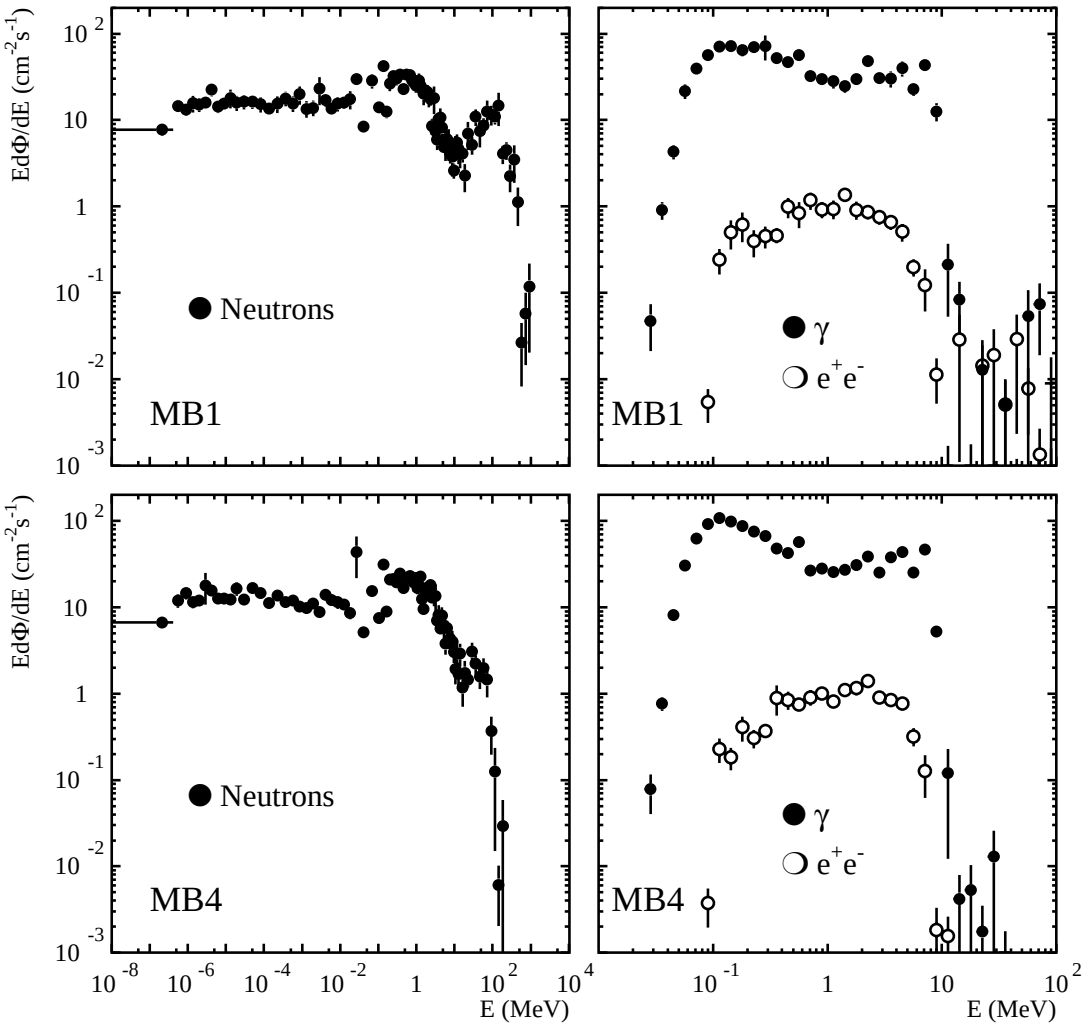


Fig. 9.53: Expected neutral particle fluence through the innermost (MB1) and the outermost (MB4) muon barrel stations.

The position resolution is reported in Fig. 9.54. No significant effect is seen, but a large increase of out of time LTRGs and a slight deterioration of the LTRG position resolution. The noise filters provided in the trigger chain are expected to cope easily with this background.

Therefore the BTI sensitivity to random single hits is low and limited to the generation of LTRG noise. Many filtering algorithms are already provided in the drift tubes local trigger design to reduce this kind of background.

9.12.2 Neutron Irradiation Studies

The radiation dose absorbed after ten years of operation at LHC is expected to be enough low to avoid significant permanent radiation damage. But on the other hand it will not be accessible, since most of it is located within the cavern, lodged on the chambers.

We expect therefore that most of the reliability of these electronics will be associated to the probability of occurrence of rare Single Events Effects (SEE) induced by the interaction of the ionizing particles with the silicon chips.

The most likely occurring SEE is called Single Event Upset (SEU). It is detected as a modification of the memory state. All memory devices (SRAMs, DRAMs, FLASH memories, microprocessors, DSPs, logic programmable state machines, etc.) are subject to such a rare event, which is caused by large energy deposition inside a sensitive node of the device. Occasionally this energy deposit can be the cause of a device latch-up: in this case the effect is destructive and the SEE cannot be recovered.

Low energy neutrons are copiously produced in the nuclear laboratories by scattering of proton or deuteron nuclei accelerators on low atomic mass nuclei targets.

The nuclear INFN laboratory of Legnaro has a 7 MV Van de Graaff accelerator. We used the reaction $^{9}Be(d,n)^{10}B$ using a thick beryllium target to generate fast neutrons, while thermal neutrons were generated using the same reaction moderating them by inclusion of the Be target in

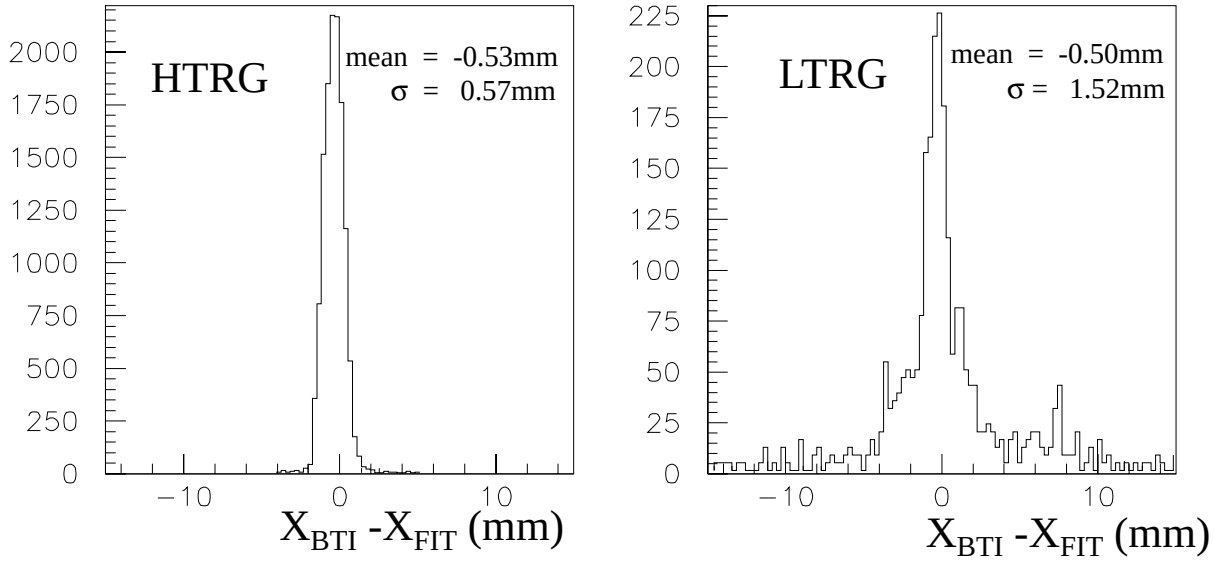


Fig. 9.54: BTI position resolution in a gamma radiation environment of 10Hz cm^2 single hit rate.

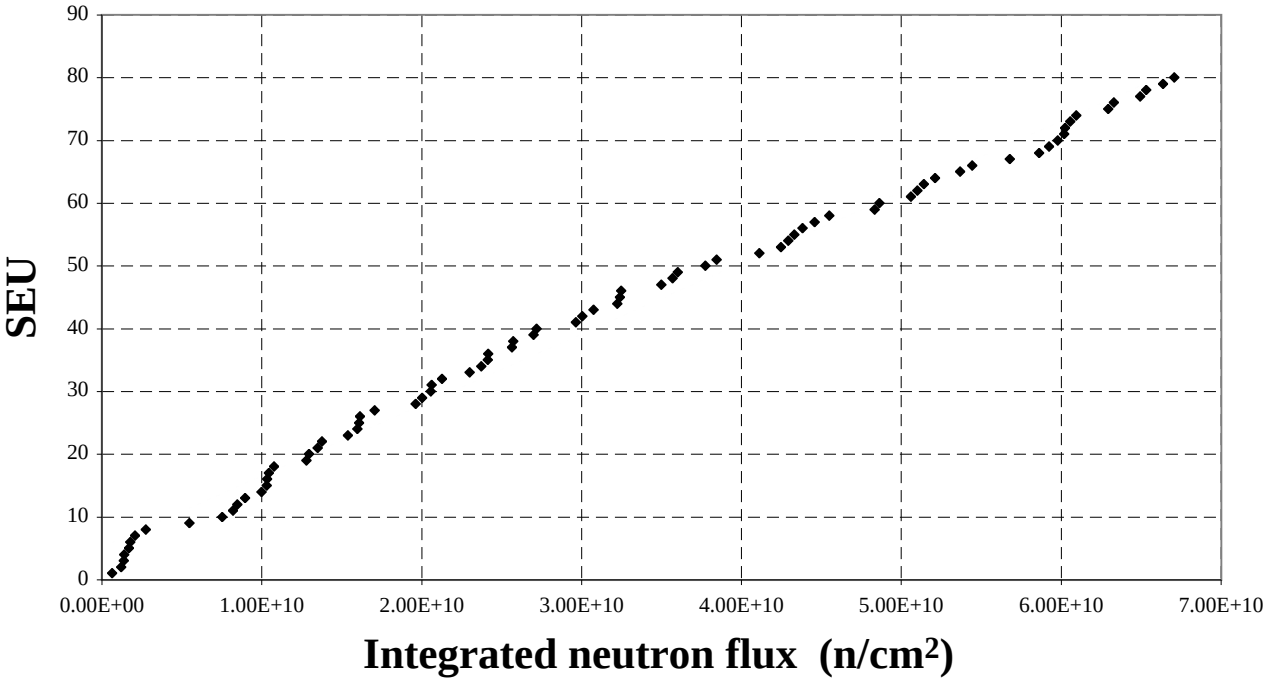


Fig. 9.55: SEU progressive number on SRAM#1 versus integrated neutron flux in the thermal neutron run. The line is the measured SEU cross section evaluation.

an heavy water tank surrounded by very thick graphite walls.The tested devices were the first prototype of the detector control board, the readout front-end board, the front-end trigger device and a prototype trigger server board.

The boards were irradiated with thermal neutrons on four data taking periods. Since the neutron flux inside the graphite is modified by the inserted boards, we had to measure the actual neutron flux on each device measuring the activation of Indium and Cadmium-Indium targets placed just in front of the integrated circuits.

The only device experiencing SEU was SRAM#1. Fig. 9.55 shows the plot of the SEU numbers versus the integrated neutron dose for all the test periods. The slope of the average line fitted in this plot is a measurement of the SEU cross section of the device. We can only quote a 90% confidence level upper limit of the SEU cross section for all the other tested integrated circuits. Indeed we had a Low Drop Regulator fault that blocked the system after integrating $7x10^9 n/cm^2$, but we feel safer quoting only the upper limit rather than the quite low SEU cross section. Results of the thermal neutron runs are summarized in Table 9.12. The error in SRAM#1 SEU cross section evaluation is essentially systematic: we quote the spread in the calculation between the four different data taking periods. The Mean Time Between Failures is computed for the whole barrel muon detector, considering the number of pieces of each chip used in the electronics layout.

There is some evidence reported in literature that the SEU cross section for fast neutron will be dependent on the neutron energy. The neutrons produced by deuteron interaction with a thick Beryllium target are not monochromatic, but measurements are nonetheless useful to give an

Table 9.12: SEU cross section and estimates of mean time between failures in the full barrel muon detectors due to thermal neutrons interactions. The limits are 90% C.L.

Component	Total rate n/cm^2	Device SEU cross section cm^2	Mean time between failures in the full detector hh:mm
LD Regulator	6.87×10^{10}	$< 1.38 \times 10^{-10}$	> 64:19
µP	6.87×10^{10}	$< 1.38 \times 10^{-10}$	> 385:56
FLASH	6.87×10^{10}	$< 1.38 \times 10^{-10}$	> 385:56
SRAM#1	6.87×10^{10}	$(1.13 \pm 0.2) \times 10^{-9}$	23:34
SRAM#2	6.87×10^{10}	$< 1.38 \times 10^{-10}$	> 192:58
EPROM	6.87×10^{10}	$< 1.38 \times 10^{-10}$	> 385:56
Optical transceiver	6.87×10^{10}	$< 1.38 \times 10^{-10}$	> 385:56
ASIC TSS	2.36×10^{10}	$< 1.38 \times 10^{-10}$	> 33:09
BTI	5.69×10^{10}	$< 1.38 \times 10^{-10}$	> 1:35

indication of the existence of fast neutrons induced SEU. Instead it is quite difficult to get the absolute SEU cross section as a function of the neutron energy.

As expected after the thermal neutron test, we had a large number of SEU from SRAM#1. The final fast neutron dose was one order of magnitude larger than the thermal neutrons one: owing to this fact we could observe SEU also on SRAM#2. Although this RAM is of the same type and belongs to the same lot, we obtained a SEU cross section two orders of magnitude lower than SRAM#1 (4 SEU after 1.52×10^{12} n/cm^2 against 135 SEU after 0.75×10^{12} n/cm^2). Thus we observed the effect reported in the existing literature of big variations for the same device.

We also had some cases of microprocessor faults: most of the cases are easily associated to corruption of the program inside the RAM and were automatically solved by automatic program reload. But in al least one case we had a complete block of the system forcing to give an external hardware reset. As for the case of the LD Regulator fault we prefer to provide a SEU cross section upper limit.

Results are collected in Table 9.13: the quoted numbers presumes that neutrons of any energy have the same probability to cause a SEU, i.e. we did not allow neither any threshold nor any energy dependence in the SEU cross section.

After the whole bunch of tests, each device had received a dose greater than 10^{12} n/cm^2, equivalent to the expected dose after more than ten years of operation at LHC. We therefore verified the status of each device after irradiation, in order to see if the neutrons had produced any

Table 9.13: Fast neutrons induced SEU estimates and upper limits. The quoted cross section assumes that any neutron in the spectrum has equal probability to cause a SEU.

Component	Total rate n/cm^2	Device SEU cross section cm^2	Mean time between failures in the full detector hh:mm
LD Regulator	9.69×10^{11}	$< 9.79 \times 10^{-12}$	> 907:42
µP	9.71×10^{11}	$< 9.77 \times 10^{-12}$	> 5457:34
FLASH	9.28×10^{11}	$< 1.02 \times 10^{-11}$	> 5214:56
SRAM#1	5.74×10^{11}	$(3.76 \pm 1.31) \times 10^{-10}$	70:54
SRAM#2	1.16×10^{12}	$(2.29 \pm 1.55) \times 10^{-12}$	14561:46
EPROM	8.46×10^{11}	$< 1.12 \times 10^{-11}$	> 4753:40
Optical transceiver	9.50×10^{11}	$< 9.99 \times 10^{-12}$	> 5336:52
ASIC TSS	1.44×10^{12}	$< 6.61 \times 10^{-12}$	> 2016:25
BTI	1.03×10^{12}	$< 9.18 \times 10^{-12}$	> 29:02

permanent damage. The only device showing a measurable deterioration was the Trigger Server ASIC (TSS), which was drawing a standby current increased by 10% with respect to the same current as measured before the tests. The final chip will be done in o.5 µm technology and we expect a significant performance improvement. Besides none of the devices underwent a latch-up SEE, but the test neutron energy (< 11MeV) could be too low to release enough energy.

A more detailed analysis can be found in [9.22].

9.13 Status and Schedule

The drift tubes local trigger schedule is shown in Fig. 9.56.

The status of each important item is as follows:

- BTI: 200 prototypes of full performance chip fully tested on bench and on beam
- TRACO: 50 prototypes of full performance chip being tested; new submission planned for 09/00
- TSS: I prototype tested on bench; full performance chip being designed
- TSM: I prototype being designed

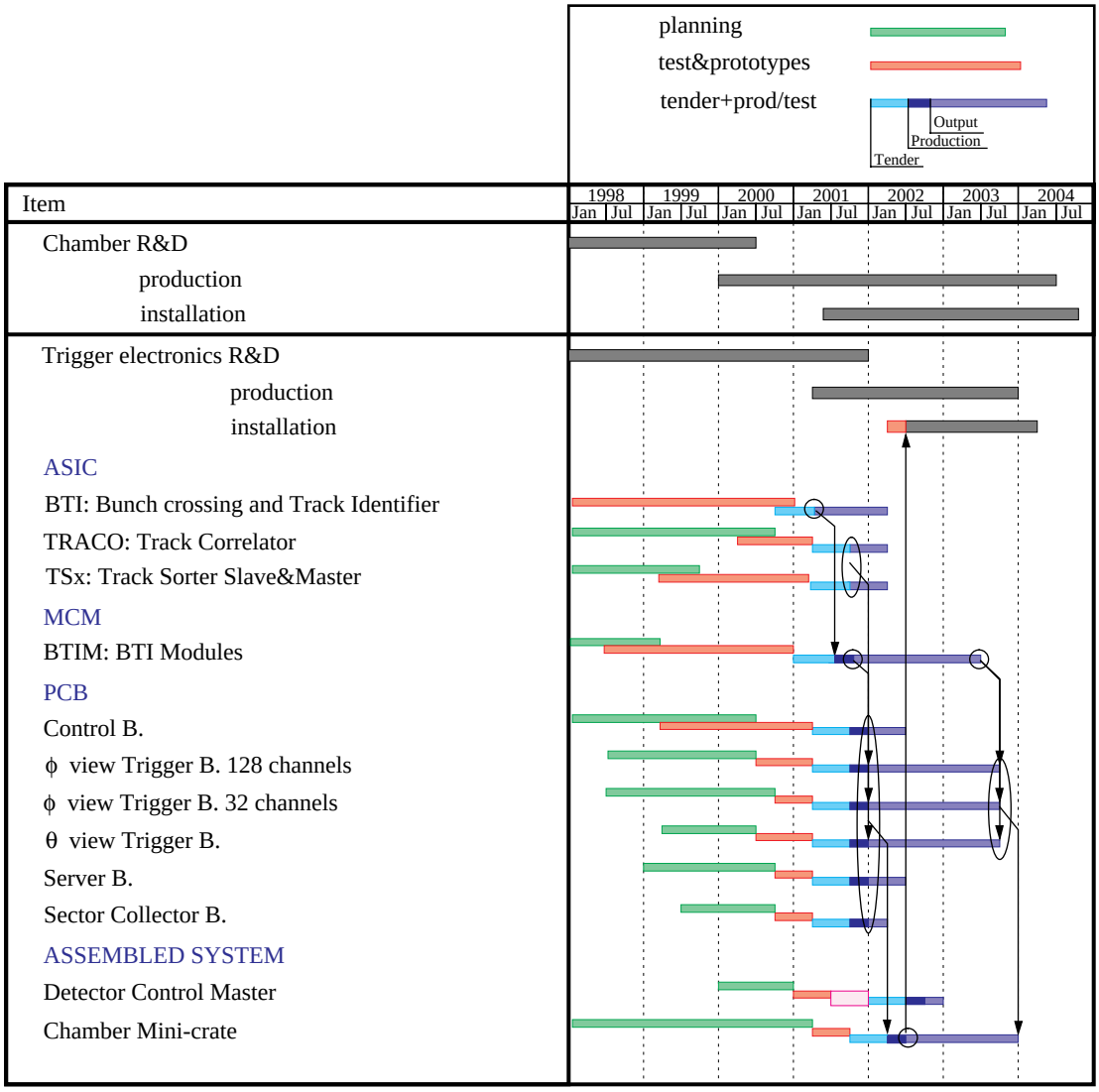


Fig. 9.56: Barrel muons local trigger schedule.

– BTIM: I prototype tested; II prototype under test
– CB: I and II prototypes tested; full performance board being designed
– PHITRB128: full performance board being tested
– PHITRB32: full performance board expected by 09/00
– THETATRB: full performance board under test
– SB: I prototype board being designed
– SCB: I prototype of Trigger optical link tested; II prototype expected by 06/00
– DTCM: full performance receiver board expected by 09/00
– Minicrate: design and aluminium profile extrusion done

Responsibility sharing between involved institutes is given in Table 9.14.

Table 9.14: Drift tubes local trigger items responsibility

Item	Institute
BTI	Padova
TRACO	Padova
TSS	Bologna
TSM	Bologna
BTIM	Padova
CB	Padova
PHITRB128	Padova
PHITRB32	Padova
THETATRB	Padova
SB	Padova/Bologna
SCB	Padova
DTCM	Padova
Minicrate	Padova/CIEMAT

References

[9.1] M. De Giorgi et al, CMS TN/95-01.

[9.2] M. De Giorgi et al, Proceedings of the First Workshop on Electronics for LHC experiments, CERN LHCC 95-96 (1995) 222.

[9.3] M. De Giorgi et al, Proceedings of the Fourth Workshop on Electronics for LHC experiments, CERN LHCC 98-36 (1998) 285.

[9.4] F. Gasparini et al, Nucl. Instr. and Meth A 336 (1993) 91.

[9.5] L. Castellani et al., "BTI User Note", http://wwweda.pd,infn.it/~rmartin/dtbx/documents/BTI_ref.ps.

[9.6] R. Martinelli et al., CMS Note/99-007.

[9.7] I. D'Antone et al, CMS TN/96-078.

[9.8] M.Kloimwieder, "Improving theη-Assignment of the DTBX Based First Level Regional Muon Trigger", CMS Note1999/054.

[9.9] CMS Note 2000/Draft, The Track-Sorter-Slave in the DTBX trigger.

[9.10] CMS Note 2000/Draft, The Track-Sorter-Master in the DTBX trigger.

[9.11] R. Cirio et al., CMS IN 2000/031.

[9.12] A. Cavicchi et al, CMS TN 96-002.

[9.13] M. De Giorgi et al, Proceedings of the Second Workshop on Electronics for LHC experiments, CERN LHCC 96-96 (1996) 22.

[9.14] M. De Giorgi et al, Nucl. Instr. and Meth A 398 (1997) 203.

[9.15] M. De Giorgi et al, Nucl. Instr. and Meth A 438 (1999) 302.

[9.16] G.M. Dallavalle et al, Proceedings of the Fourth Workshop on Electronics for LHC experiments, CERN LHCC 98-36 (1998) 291.

[9.17] G.M. Dallavalle et al, Proceedings of the Fourth Workshop on Electronics for LHC experiments, CERN LHCC 98-36 (1998) 294.

[9.18] CMS IN 2000/Draft Pattern Unit for high throughput device testing

[9.19] C.Grandi, Proceedings of the International Conference on Computing in High Energy Physics and Nuclear Physics (CHEP2000), Padova, Italy, page 220.

[9.20] M. Passaseo et al.,Nucl. Instr. and Meth A 367 (1999) 418.

[9.21] CMS, The Muon Project, Technical Design Report, CERN/LHCC 97-32.

[9.22] S. Agosteo et al, CMS Note 2000/024