TTCrx Reference Manual

A Timing, Trigger and Control Distribution Receiver ASIC for LHC Detectors

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Chapter 1

Introduction

The TTCrx is a custom IC that was designed by the CERN ECP Microelectronics group. It acts as an Interface between the Timing Trigger and Control Distribution (TTC) system for LHC detectors and its receiving end users. The ASIC receives control and synchronisation information from the central TTC system and makes it available to the front-end electronics controllers in the detectors. The TTCrx can be programmed to compensate for particle times of flight and for propagation delays associated with the detectors and their electronics. The IC delivers the LHC timing reference signal, the first level trigger decisions and its associated bunch and event numbers. Besides, it provides for transmission of synchronised broadcast commands and individually-addressed controls and parameters.

This document is intended to provide a functional and physical description of the TTCrx IC from the user perspective.

TTC SYSTEM OVERVIEW

The Timing Trigger and Control (TTC) system for LHC detectors has been specified and complete descriptions of the system and its functionality can be found in references [1] and [2]. However, a brief overview of the TTC system features that are most relevant for the understanding and utilisation of the TTCrx IC is made here.

In each LHC experiment the TTC system controls the detector synchronisation and delivers to the front-end electronics controllers the fast signals and messages that are necessary to run the experiments. Figure 1 Illustrates the basic architecture of the TTC system: at the top of the TTC tree structure, two communication channels are Time Division Multiplexed (TDM), BiPhase Mark (BPM) encoded and transmitted

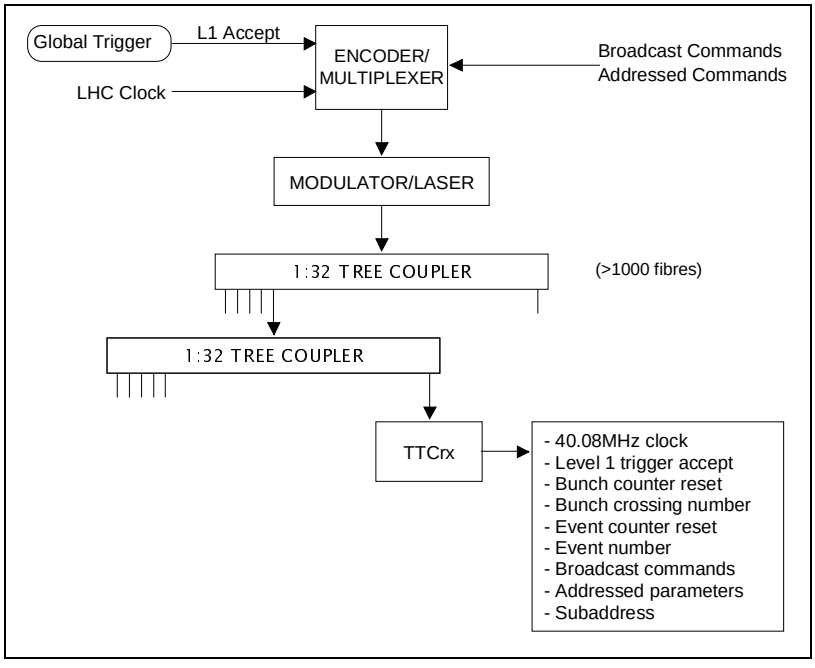

Figure 1 TTC optical distribution network

over a passive optical fibre distribution network using a single laser source. One of the TDM channels (channel A) is exclusively dedicated to broadcast the first-level trigger-accept (L1A) decisions, delivering a one-bit decision for every bunch crossing. The other, (channel B) is used to broadcast data to all or specific system destinations. The TTC system is also used to distribute the LHC 40.08 MHz bunch-crossing reference clock signal. This signal is not explicitly transmitted over the network and has to be recovered from the incoming data at each TTC system destination.

Data in channel B can be of two types [1], [2]: broadcast commands or individually addressed data/commands. Broadcast commands are used to distribute messages to all TTC destinations in the system. When detected, these commands are executed by all the TTC receivers. The individually addressed data/commands are implemented in the system to transmit user-defined data and commands over the network. These commands have two distinct modes of operation. In the first mode, they are aimed at the TTC receivers themselves and their user-defined content is used to control the receiver's operation. In the second mode, the data are intended for the external electronics. In this case, both the data and sub-address contents of the received commands are made externally available by the addressed TTC receiver.

Both the broadcast and the individually addressed commands are transmitted over the TTC network using a frame format that has been specified in reference [1] and which is schematically represented in Figure 2. The frame structure contains several fields to control the transmission and includes a field in which several redundant bits are inserted for error detection and correction. The coding scheme used is a standard Hamming code with the capability of double error detection and single bit error correction. The error correction coding covers the 8-bit data word in the case of a broadcast command/data frame and the 32-bit data in the case of an individually-addressed command/data frame[1]. The address space selection bit (E) instructs the addressed TTC receiver either to execute an internal operation or to make the received individually addressed command/data externally available. Using this scheme it is possible to address up to 256 internal and external subaddresses associated with up to 16K timing receivers in each timing distribution group.

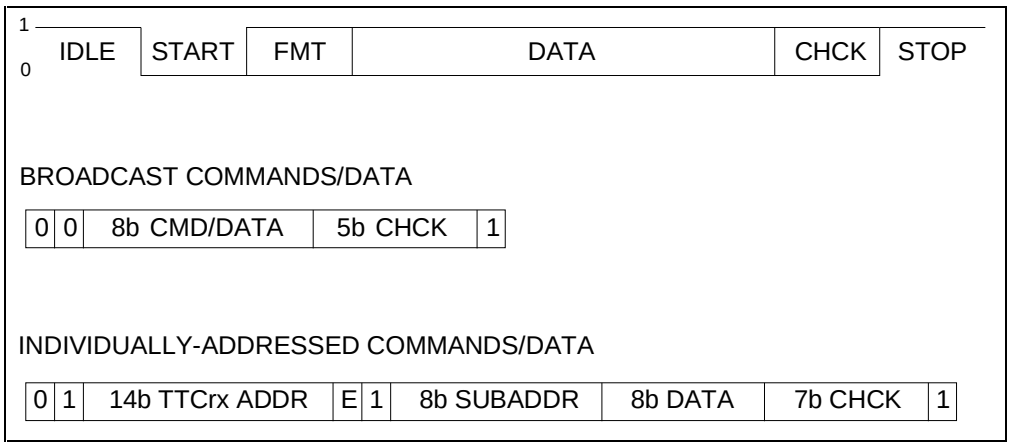

Figure 2 Data transmission frame format

Each frame is identified by a header bit (FMT) which indicates its type. Start (logical "0") and stop (logical "1") bits are always included at the beginning and end of the frame transmission to facilitate correct synchronisation.

[1]Start, frame type and stop bits are not included in the error correction scheme.

As mentioned before, channels A and B are time division multiplexed and biphase mark encoded before transmission over the network. With this type of encoding there is a fundamental phase ambiguity between the recovered clock and the two transmitted channels. This ambiguity is resolved automatically in the receivers by monitoring constraints imposed on the channel A data structure. Figure 3 shows the TTC signal encoding for the two TDM channels.

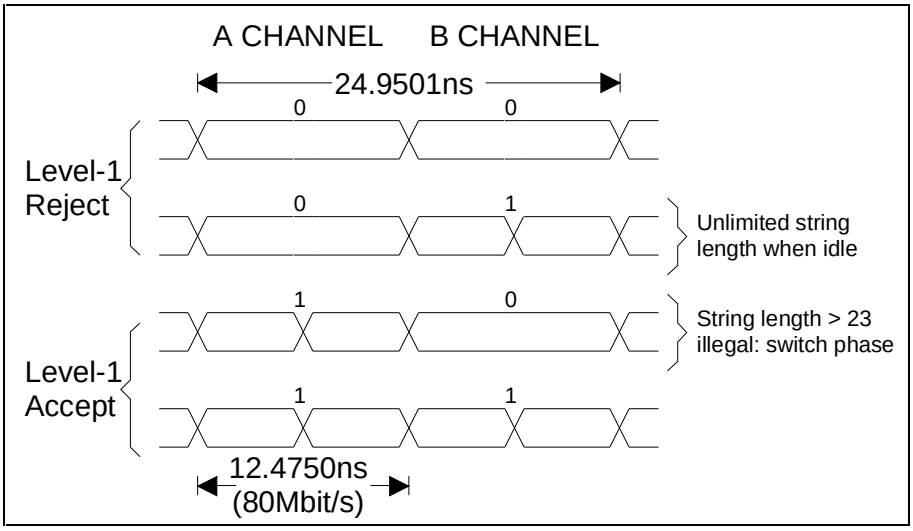

Figure 3 TDM biphase mark encoding

TTCrx OVERVIEW

A timing receiver is associated with each of the outputs of the TTC optical distribution network. Each receiver is composed of a commercial integrated photodetector-preamplifier and of the special purpose custom IC (TTCrx) described in this manual [3]. The TTCrx ASIC receives, decodes, executes and distributes the commands and data broadcast over the TTC distribution network. It recognises individually addressed commands for purposes of internal and external control and supports the transmission of synchronised broadcast commands. One of the main functions of the TTCrx is to recover and distribute the 40.08 MHz LHC reference clock with minimum jitter. The timing receiver makes also available to the detector electronics the first-level trigger-accept decisions and their associated bunch crossing and event identification numbers. Each TTCrx IC is identified in the distribution network by a unique 14-bit channel Identification (ID) number. This number is read from a serial PROM at power up or after a reload ID broadcast command is received. The ASIC control logic identifies the A and B channels, deserializes the data in the B channel and continuously monitors it to look for the presence of its ID channel number.

The TTCrx IC has been mapped into a standard 1μm CMOS digital process from ES2 with all the analogue and time-critical functions implemented in full custom. Standard cells were used to implement the digital and the non time-critical functions. The ASIC footprint is 4.5×4.5mm and has been packaged in a 100 pin PGA package.

TTCrx architecture

Figure 4 shows the architecture chosen to implement the TTCrx functionality. As shown in this figure, the ASIC receives the TTC system data in the form of an electrical signal from the optical preamplifier. Due to the optical power levels

detected by the preamplifier, this signal needs to be amplified to CMOS levels before it can be used for clock recovery, data decoding and demultiplexing. The unit marked as “Linear Receiver” in Figure 4 implements that function. Signal level detection and automatic gain control are also taken care of inside this block. After the signal is restored to CMOS levels, it is fed to the “Clock Extraction” and the “Data Decoder/Demultiplexer” units where the LHC system clock is recovered with minimum jitter, and the trigger (A) and data (B) channels are separated. The recovered clock is then fed to the “Programmable Fine Deskew” unit where two different clock phases, synchronous with the LHC system clock, are generated. The phases of the two clocks can be controlled independently via commands on the B channel. The “Programmable Fine Deskew” unit allows the two clock phases to be changed in steps of 104 ps between 0 and 25 ns.

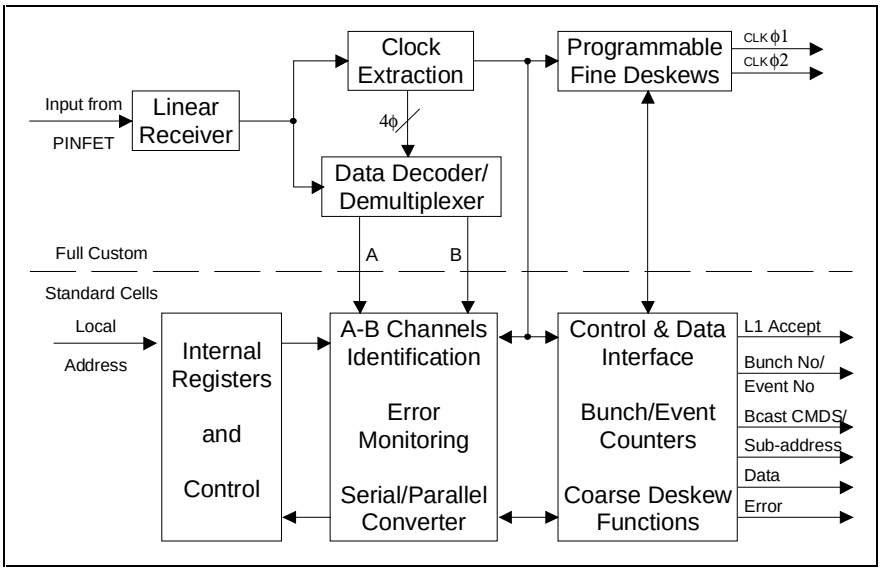

Figure 4 Timing receiver block diagram

The TTCrx control logic consists of three major blocks. The first block contains the internal configuration and status registers and implements the logic necessary to read a 14 bit number from an external serial configuration PROM that supplies the TTCrx ASIC with its unique system address.

The second block identifies the trigger and data channels and constantly monitors the data in channel B for transmission errors. It deserializes the received data and decides if this is addressed to the IC itself or to some external addressable or common space. Finally, the third functional block implements two independently programmed coarse deskewing functions for the first-level trigger signal and the broadcast commands. The related control registers can be programmed by individually addressed data transmitted over the B channel. Both first-level trigger and broadcast commands can be deskewed over a range of 16 bunch-crossing intervals.

TTCrx internal registers

The TTCrx contains several internal registers used for control and monitoring of its operation. These registers are:

- Configuration register;
- Control register;
- Coarse Delay register;

- Fine Delay registers;
- Bunch Counter;
- Event Counter register;
- Single Bit Error;
- Double Bit/Frame Error counter.

The **Configuration** register contains the configuration bits read during initialisation from the external serial PROM. It is used to store the 14-bit chip ID and to set up some of the different ASIC operation and test modes.

The **Control** register is used to minimise the IC power consumption by allowing the disabling of some of the chip functionality in applications that do not require it. For instance, the Event and Bunch counters and the Address and Data buses can be disabled if not required by the external electronics.

The **Coarse Delay** register holds the deskewing parameters for the First Level Trigger Accept (L1A) and the Bunch Counter Reset signals. The contents of this register in conjunction with that of the Fine Delay register affects the total amount of deskewing. Since the same deskewing is applied to the L1A signal and the broadcast commands, deskewing of the latter ones will also have to be performed at the source of the TTC system to compensate for the time necessary to transmit and decode these commands.

The **Fine Delay** registers hold the deskewing parameters that control the programmable delay generator discussed previously. When combined with the coarse deskewing functions, a compensation range of 16 bunch-crossing intervals is obtained. This allows a substantial margin beyond the possible maximum variations due to differences in time-of-flight and optical fibre path lengths in the detectors.

The **Bunch** and the **Event Counters** are free running counters that are incremented by the recovered clock and the L1A signals, respectively. These counters can be reset by specially defined broadcast commands. The Bunch Counter register content, which is a 12-bit number, is normally available to the outside logic. However, during the two clock cycles following a trigger accept, the 24-bit Event Number register content can optionally be made available to the outside electronics on the same 12 output lines.

Finally, the **Single Bit Error** and the **Double Bit/Frame Error counters** are used to keep track of the number of errors occurring during data reception. Since the receiver Hamming decoder is capable of fully recovering from single bit errors, the data are accepted after correction and the Single Bit Error register incremented. When a double bit error is recognised by the receiver logic or a frame error is detected, the data are ignored and the contents of the Double Bit/Frame Error register incremented. The contents of the internal error counters are dumped on the external data bus when an error dump broadcast command is issued by the central TTC system.

Chapter 2

TTC System Frame Formats

This chapter discusses the frame formats used for transmission of broadcast commands and individually addressed commands/data in the TTC system. This topic has been introduced in section "TTC system overview" of chapter 1.

FRAME FORMATS

Two basic frame formats are used to transmit broadcast commands and individually-addressed commands/data to the TTC receivers. The frames are sent with several redundant bits for single bit error correction and double bit error detection. The coding scheme used is a standard Hamming code with one additional even parity bit to detect double bit errors [4]. A start and a stop bit are included in each frame for correct frame synchronisation. The two adopted frame formats are defined as follows:

Broadcast frame

The broadcast frame is used to distribute messages to all TTC receivers in the system (broadcast commands). This type of frame is identified by a "0" in its header bit (FMT). All TTCrxs, after having performed appropriate checking on the received packet, execute the operation requested in the data part of the frame. For broadcast frames, error correction and detection are made on the 8 data bits.

START	FMT	CMD/DATA <7:0>	CHCK <4:0>	STOP
0	0	dddddddd	eeeee	1

Individually-addressed commands/data frame

Individually-addressed commands/data frames are identified by a "1" in the header bit (FMT). This frame is used to address a single TTCrx in the system[2]. Data sent to a particular TTCrx are output to the data bus and the Data Qualifier <3:0> bus is set to "0" to validate the data bus content. The error correction coding covers the entire 32 data bits in the frame. Start, header and stop bits are not included in the error correction scheme.

START	FMT	TTCrx ADDR <13:0>	E	1	SUBADDR <7:0>	DATA <7:0>	CHCK <6:0>	STOP
0	1	ttttttttttttt	i	1	ssssssss	dddddddd	eeeeeee	1

[2]See "TTCrx Addressing" for exception on the TTCrx ADDR "0".

Chapter 3

Receiver Addressing

This chapter discusses the different receiver addressing modes implemented in the TTC distribution system and recognised by the TTCrx ASIC.

TTCrx ADDRESSING

Each TTCrx IC is identified in the distribution network by a unique 14-bit channel Identification (ID) number. This number is read from a serial PROM[3] at power up or after a reload ID broadcast command is received. Each TTCrx in the distribution system deserializes the data in channel B and continuously monitors it to look for the presence of its ID channel number.

Individual addressing

The individually addressable space for each TTCrx is split into two: internal and external. The internal address space is used to write in the TTCrx internal registers while the external space allows commands and data to be transmitted to the detectors electronics. When an individually-addressed commands/data frame[4] is received with the bit E equal to "0" the internal address space is assumed. A "1" received in the E bit indicates external addressing and the external subaddress and data buses are set according to the data contents of the received command.

The TTCrx **internal addressing space** is allocated as follows:

SUBADDR <1:0>	Location
00000000	Fine Delay Register 1 <7:0>
00000001	Fine Delay Register 2 <7:0>
00000010	Coarse Delay Register <7:0>
00000011	Control Register <7:0>

Global addressing

Simultaneous addressing of all the receivers in a TTC distribution group is made using broadcast commands. Every TTCrx in a distribution group should execute the received command. In addition to the broadcast addressing provided by the broadcast frame[5], another method of sending data to all TTCrxs is provided by reserving the lowest TTCrx address (i.e. ADDR<13:0> = "0") to mean a broadcast message with 8 bit of data to all chips. The external/internal bit (E) and the subaddress range still remain active for this message type.

[3]Serial PROM type XC1736 from Xilinx [5].
[4]See "Frame formats" for individually-addressed command/data frame specification.
[5]See "Frame formats" for broadcast frame specification.

Chapter 4

Receiver Internal Registers

In this chapter, the TTCrx internal registers are described in detail. A brief summary of the TTCrx registers and their functionality can be found in section “TTCrx overview” of chapter 1.

TTCrx REGISTERS

The TTCrx contains several internal registers for control and monitoring of its operation. These registers are listed below:

- Configuration register;
- Control register;
- Coarse Delay register;
- Fine Delay registers;
- Bunch Counter register;
- Event Counter register;
- Single Bit Error counter;
- Double Bit/Frame Error counter.

Configuration register

This 66 bit register contains the string of configuration bits read at initialisation time from the external serial PROM. It is used to store the 14-bit chip ID and to set up some of the different ASIC operation and test modes. The register is not directly readable but it can be dumped on the external data bus after reception of a CRDUMP broadcast command. If this instruction is executed, the register is dumped onto the data bus in a sequence of bytes, starting from the lowest one (bits 7 to 0). The **configuration register** bit allocation is as follows:

PROM bit(s)[6]	Function/internal signals	Recommended parameters
65-61	aux_mux_select<4:0>	“00001”
60	enable_reinitialise	User defined
59	dll_input_mux	“0”
58	dll_reset_mux	“0”
57-53	dll_isel_b<4:0>	“11110”
52-49	lock_period<3:0>	“1111”
48-45	check_period<3:0>	“1111”
44-43	vco_isel<1:0>	“01”

[6] Bit aux_mux_select<4> is the first bit to be read from the serial PROM and bit ID<0> the last.

42-38	pfd_isel_b<4:0>	“11101”
37-33	pd_isel_b<4:0>	“11101”
32	start_ref_gen_b	“1”
31-27	dll_isel_b<4:0>	“11101”
26-24	aux_mux<2:0>	“000”
23	decode_mux	“0”
22	pll_mux	“0”
21	ref_gen_mux[7]	“0”
20-16	amp_isel_b<4:0>	“10000”
15	Enable Clock40Des2	User defined
14	Enable Hamming decoding	“1”
13-0	TTCrx ID<13:0>	User defined

With the exception of the user defined parameters, the configuration register recommended parameters should never be modified by the user.

Control register

The control register is used to minimise the IC power consumption by allowing the disabling of some of the chip functionality in applications that do not require it. Several bits are available in the **control register** and they are allocated as follows:

	Function	Reset state
0	Enable Bunch Counter operation	1 (enabled)
1	Enable Event Counter operation	1 (enabled)
2	Reserved	
3	Enable Single Bit Error Init.	0 (disabled)
4	Enable Double Bit Error Init.	0 (disabled)
5	Enable Parallel A/D bus[8]	0 (disabled)
6	Enable Serial A/D bus	0 (disabled)
7	Enable non-deskewed 40 MHz output	1 (enabled)

Bits 3 and 4 are used to control the re-initialisation process. If receiver re-initialisation is enabled in the configuration register then, bits 3 and 4 control the re-initialisation conditions.

Coarse delay register

The Coarse Delay register holds the deskewing parameters for the First Level Trigger Accept (L1A) and the Bunch Counter Reset signals. The content of this register in conjunction with that of the Fine Delay register affects the total amount of deskewing applied to these signals. Since the same deskewing is applied to the L1A signal and the broadcast commands, deskewing of the latter ones will have also to

[7] This bit must be set to “1” if by-passing” of the post-amplifier is required. In this case, the TDM biphase mark signal should be provided to the A_test0 input. This input requires CMOS levels for correct operation.

[8] Setting this bit forces to “0” the following output pins: Dout<7:0>, DQ<3:0>, SubAddr<7:0> and DoutStr . All the other outputs function normally.

be performed at the source of the TTC system to compensate for the time necessary to transmit and decode these commands.

The 8 bit **coarse delay register** holds two sets of four bits, each determining the coarse deskewing of two groups of registers. The coarse delay register bits <3:0> and <7:4> control the amount of deskewing applied to the external strobe signals BrcstStr1 and BrcstStr2 respectively.

Bits	Deskewing function
<3:0>	Bunch counter reset (deskew 1)
<7:4>	User broadcast command (deskew 2)

Fine delay registers

Two 40.08 MHz clock outputs are provided by the TTCrx. These outputs are controlled by two separate registers. The fine delay registers are loaded by sending data to them using an individually-addressed commands/data frame addressed to locations “0” and “1” in a given TTCrx. These are 8 bit registers allowing the clock phase to be changed in steps of 104 ps between 0 and 25 ns.

Notice that the mapping of the eight bits in a linear delay requires a mapping table which will be provided as a software subroutine.

Bunch counter

The bunch counter is a free running counter incremented by the received clock signal. This counter is 12 bit long and is reset uniquely by the BCRST broadcast command and by the chip initialisation procedure.

Event counter

The event counter is a free running counter incremented by the L1Accept signal. This counter is 24 bit long and is reset uniquely by the ECRST broadcast command and by the chip initialisation procedure.

Single bit error counter

This 16 bit counter keeps track of the number of single bit errors recognised by the receiver’s Hamming decoder. Since these errors are fully recovered, received commands and data are accepted by the TTCrx after correction in the receiver block itself.

Double bit error and frame error counter

This 16 bit counter keeps track of the number of double bit errors recognised by the receiver logic and of the number of frame errors (stop bit not equal to one). After such an error, received data are not used and no action is taken. The TTCrx tries to resynchronise to the next start bit. In the process of resynchronisation, errors can again occur.[9]

[9] Note that both the single error counter and double bit and frame error counter are disabled once their content reaches 65535. A re-initialisation sequence is necessary to reactivate and reset these counters.

Chapter 5

Broadcast Messages

This chapter describes the system and user defined broadcast commands/data.

BROADCAST COMMANDS/DATA

The TTCrx can accept up to 256 different broadcast messages, encoded in the 8 bit broadcast packet. Broadcast messages are deskewed by a delay equal to the coarse delay programmed in the Coarse Delay register bits <3:0>. Since this delay also affects the L1Accept signal, deskewing of the broadcast commands will also have to be performed at the source of the TTCrx system to compensate for the time necessary to transmit these commands.

The most common broadcast commands are enumerated below:

Command	Format #	Function
NOP	uu ssss 00	Do nothing[10]
BCRST	uu ssss 01	Bunch counter reset
ECRST	uu ssss 10	Event counter reset
EBCRST	uu ssss 11	Reset event and bunch counters
ERDUMP	uu 0001 bb	Dump internal error counter to Data Bus
CRDUMP	uu 0010 bb	Read PROM to Data Bus[11]
RESERVED	uu 0011 bb	
INIT	uu 0100 bb	Reload TTCrx ID and re-initialise
USER	uu xxxx bb	User defined broadcasts[12]

The “uu” bits in the table indicate user defined broadcast messages. The four “ssss’” bits are used for system wide broadcast messages. Some of these messages are already defined in the table (ERDUMP, CRDUMP, INIT). The detailed operation of each of the above instruction is explained below.

BCRST

Bunch counter reset: a bunch counter reset is performed.

EBCRST

Event and bunch counter reset: an event and bunch counter reset is performed.

[10] Used for testing purposes.
[11] See “Configuration register” for detailed explanation of the dump sequence.
[12] The broadcast packet is written to broadcast bus

ECRST

Event counter reset: an event counter reset is performed.

ERDUMP

Error dump: the internal error counters are dumped on the external data bus. For this operation the data qualifier bits are used as follows:

DQ	Data bus content
0001	Single Bit Error Counter High
0010	Single Bit Error Counter Low
0011	Double Bit Error Counter High
0100	Double Bit Error Counter Low

Data are output in the external data bus in consecutive clock cycles. As for a normal data transfer, the data strobe line (DoutStr) signals the presence of valid data on the bus and the DQ bits indicate the current status in the error dump sequence.

CRDUMP

Configuration register dump: The internal configuration and control registers are dumped on the external data bus. For this operation the data qualifier bits are used as follows:

DQ	Data bus content
0101	Fine Delay register 1
0110	Fine Delay register 2
0111	Coarse Delay register
1000	Control register
1001	Configuration register bit <7:0>
1010	Configuration register bit <15:8>
1011	Configuration register bit <23:16>
1100	Configuration register bit <31:24>

INIT

This instruction performs a warm re-initialisation of the TTCrx. Since in order to be recognised, this instruction requires a working analogue front end, re-initialisation is limited to the digital part of the TTCrx (no PLL re-initialisation).

USER

User defined command: this instruction sets the two user defined external broadcast pins to the data received in the user defined part of a broadcast command.

Chapter 6

Receiver Operation

TTCrx OPERATION

Reset sequence

To initialise the TTCrx after a power on, the reset_b pin is activated. This is an active low signal which reinitialises the TTCrx completely. Upon completion of the initialisation sequence the TTCrx activates the TTCReady signal. The external reset signal forces the TTCrx to go through a complete re-synchronisation sequence and reloads all the system parameters from the serial PROM. The resynchronisation sequence can take up to 25 μsec.

A TTCrx cold re-initialisation is performed every time the internal PLL lock signal is lost.

INIT sequence

A warm re-initialisation sequence is performed each time a INIT broadcast command is received. The re-initialisation sequence is limited to the digital part of the TTCrx. During execution the external serial PROM is read, channels A and B identified, and frame synchronisation acquired. At the end of the re-initialisation the TTCReady pin is asserted.

L1A sequence

On reception of an L1Accept signal on the A channel, the TTCrx outputs the following sequence of signals on the respective pins:

Control Register, bit <1:0>	Cycle	Sequence
11	0	Event counter low on bunch counter bus
	1	Event counter high on bunch counter bus
	2	Bunch counter on bunch counter bus
01	0	Bunch counter on bunch counter bus
10	0	Event counter low on bunch counter bus
	1	Event counter high on bunch counter bus
00	0	Event counter low on bunch counter bus

The number of cycles depends on the setting of the two low bits in the control register, as explained in “Control register”.

Broadcast sequence

The content of the received broadcast command is output on the broadcast bus (Brcst<7:2>). The strobe lines BrcstStr1 and BrcstStr2 are activated (for a clock period) after the delays specified in the coarse delay register have elapsed.

Data sequence.

Upon reception of an individually-addressed commands/data frame, its data content is output on the data bus (Dout<7:0>) and its subaddress content on the subaddress bus (SubAddr<7:0>). The data qualifier bits (DQ<3:0>) are set to “0” to indicate data transmission and the data strobe line (DoutStr) is set to indicate valid data during a clock cycle. When the received command is intended for the internal addressing space the strobe line DoutStr is not activated and the contents of the data and subaddress buses remain unchanged.

TTCrx configuration

In order to adapt the operation of the TTCrx to different environments, several optional features can be programmed after reset by reading an external serial PROM. The TTCrx uses three dedicated pins (PromReset, PromClk and PromD) to implement a serial protocol identical to the one used in devices such as the Xilinx 1736 or equivalent. The user is referred to the data sheets of this product for detailed information [5].

In addition to containing configuration parameters, the serial PROM is also used to store testing parameters. These parameters have been specified in section “TTCrx registers”. ***With the exception of the user defined parameters, the configuration register recommended parameters should never be modified by the user.***

Chapter 7

TTCrx Signals and Timing

This chapter describes the TTCrx external signals and the most important timing relations among these signals.

TTCrx EXTERNAL SIGNALS

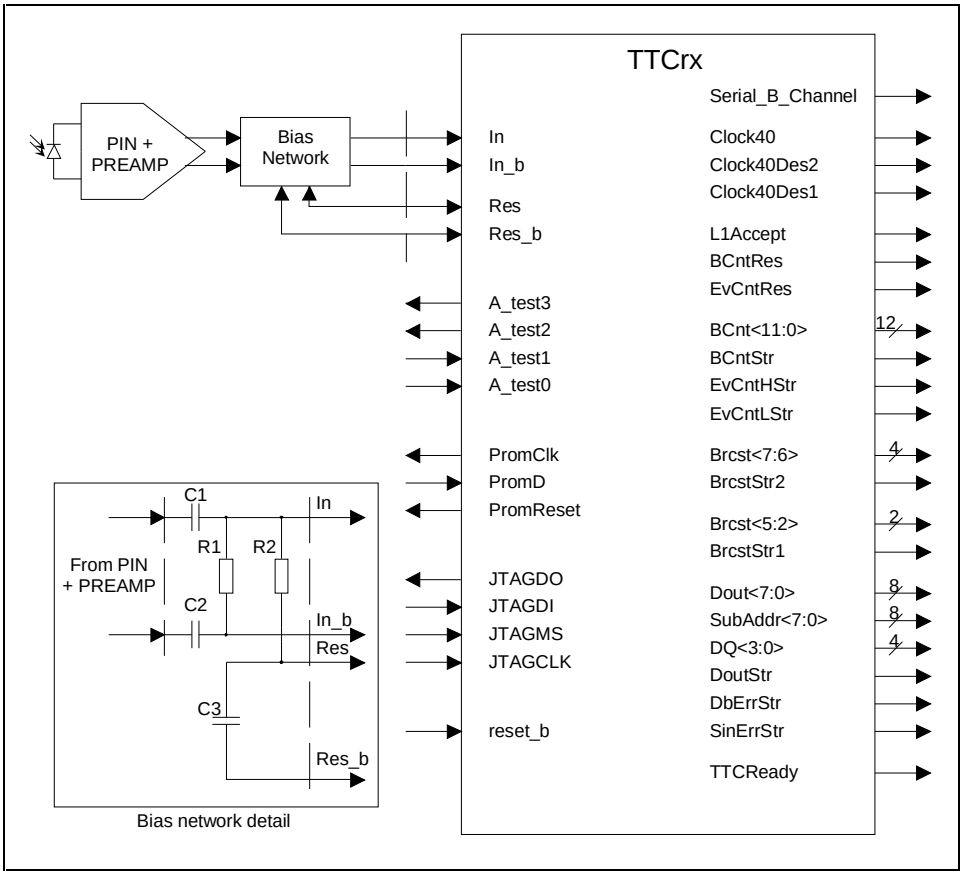

Figure 5 TTCrx external signals and analogue inputs bias arrangement.

The TTCrx signals available to the user and the bias arrangement required for interfacing with the photodetector-preamplifier are represented in Figure 5. A description of the functionality of each individual signal is given next.

TTCrx signals

A_test0

Full custom circuit test input.

A_test1

Standard cells circuit test input.

A_test2

Full custom circuit test output.

A_test3

Standard cells circuit test output.

BCnt<11:0>

Bunch counter output bus. This bus usually reflects the content of the bunch counter register. After a first level trigger accept decision it can be optionally used to provide the event number. Its mode of operation is controlled by the control register and its data type is validated by the signals BCntStr, EvCntHStr and EvCntLStr.

BCntRes

Bunch counter reset signal. Indicates a bunch counter reset. As the L1Accept signal, its deskewing is controlled by bits <3:0> in the coarse delay register and by the content of the fine delay register with subaddress “0”. See “Coarse delay register” and “Fine delay registers".

BCntStr

Bunch counter strobe. Indicates that a bunch number is present on the output BCnt<11:0> bus.

Brcst<7:6>

Broadcast commands/data output bus. User defined part of a broadcast message. See “Broadcast commands/data”.

Brcst<5:2>

Broadcast commands/data output bus. System wide part of a broadcast message. See “Broadcast commands/data”.

BrcstStr1

Broadcast messages strobe 1. The total amount of deskewing applied to this strobe signal is controlled by bits <3:0> of the coarse delay register. (see “Coarse delay register”).

BrcstStr2

Broadcast messages strobe 2. The total amount of deskewing applied to this strobe signal is controlled by bits <7:4> of the coarse delay register. (see “Coarse delay register”).

Clock40

LHC 40.08 MHz non-deskewed reference clock signal. This output can be enabled/disabled by writing into the “control register”.

Clock40Des1

LHC 40.08 MHz deskewed reference clock 1. The deskewing factor is controlled by writing into the TTCrx subaddress “0” (see “Fine delay registers”).

Clock40Des2

LHC 40.08 MHz deskewed reference clock 2. The deskewing factor is controlled by writing into the TTCrx subaddress “1” (see “Fine delay registers”).

DbErrStr

Double error or frame error strobe. Indicates that a double error or a frame error has occurred.

Dout<7:0>

Data bus. This bus is normally used to output the data content of an individually-addressed commands/data. However, it is also used for dumping the contents of the internal error counters and of the configuration register (see “ERDUMP” and “CRDUMP”). The type of data present in the bus is validated by signals DQ<3:0>. Bus operation can be enable/disabled by writing into the control register.

DQ<3:0>

Data qualifier bits. This bus indicates the type of data present on the data bus. register (see “ERDUMP” and “CRDUMP”).

DoutStr

Data out strobe. Indicates valid data on the data bus.

EvCntHStr

Event counter high word strobe. Indicates that the output bus BCnt<11:0> contains the high word of the event number.

EvCntLStr

Event counter low word strobe. Indicates that the output bus BCnt<11:0> contains the low word of the event number.

EvCntRes

Event counter reset signal. Indicates an event counter reset. As the L1Accept signal, its deskewing is controlled by bits <3:0> in the coarse delay register and by the content of the fine delay register with subaddress “0”. See “Coarse delay register” and “Fine delay registers

In and In_b

Differential analogue input. Signals **In** and **In_b** interface with the photodetector-preamplifier using the bias network detailed in Figure 5. Correct operation of the TTCrx IC requires the peak to peak amplitude of the input differential signal to be within 5 mV_{pp} and 2 V_{pp}. The input signal has to be BiPhase Mark encoded (see “TTC system overview”) and the frame formats specified in sections “TTC system overview” and “Frame formats” have to be respected for correct receiver operation.

JTAGCLK

Not implemented in the current version of the TTCrx IC.

JTAGDI

Not implemented in the current version of the TTCrx IC.

JTAGDO

Not implemented in the current version of the TTCrx IC.

JTAGMS

Not implemented in the current version of the TTCrx IC.

L1Accept

First level trigger-accept signal. The total amount of deskewing applied to this signal is controlled by bits <3:0> in the coarse delay register and by the content of the fine delay register with subaddress “0”. See “Coarse delay register” and “Fine delay registers".

PromClock

Serial configuration PROM clock signal. See “Individual addressing”, “Configuration register” and reference [5].

PromD

Serial configuration PROM reset signal. See “Individual addressing”, “Configuration register” and reference [5].

PromReset

Serial configuration PROM data output. See “Individual addressing”, “Configuration register” and reference [5].

reset_b

Active low reset signal. See “Reset sequence”.

Res an Res_b

Analogue input bias. See inset in Figure 5 for details on the bias circuit.

Serial_B_Channel

This signal is used to make available to the users the serial data received on channel B (including frame, start and stop bits) The bit rate is 40.08 Mbit/s. This output can be enabled/disabled by writing into the control register.

SinErrStr

Single error strobe. Indicates that a single error has occurred.

SubAddr<7:0>

Subaddress bus. Used to output the subaddress content of an individually address commands/data. Bus operation can be enable/disabled by writing into the control register.

TTCReady

TTCrx ready.

TTCrx TIMING

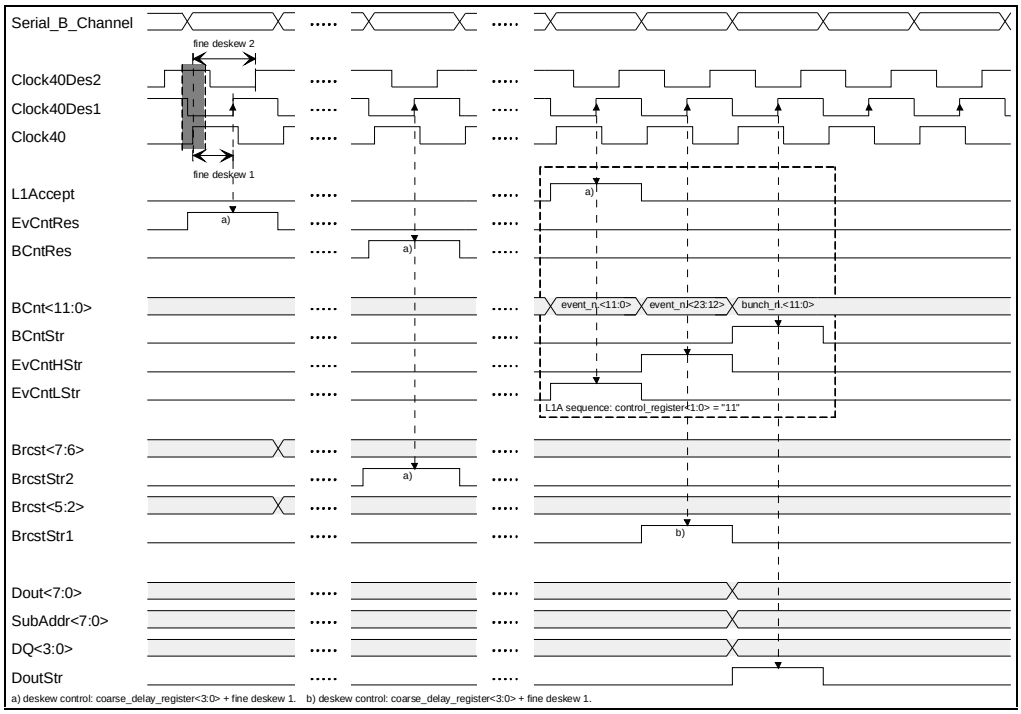

Figure 6 TTCrx timing

The general timing relations among the TTCrx output signals are illustrated in Figure 6. The timing relations among some of these signals can be modified by the user. The internal registers that control the TTCrx timing are: the coarse delay register and the fine delay registers 1 and 2. The contents of this registers can be modified using individually-addressed commands/data as explained in sections “TTCrx registers” and “Broadcast commands/data”

Chapter 8

TTCrx Packaging and Pin Assignments

TTCrx PACKAGING (PRELIMINARY)

The first version of the TTCrx has been package in an 100 pin PGA package. However, the final version of the TTCrx IC will be packaged as a compact (15×15mm) Ball Grid Array.

The pin positions for the **PGA100** package is given below:

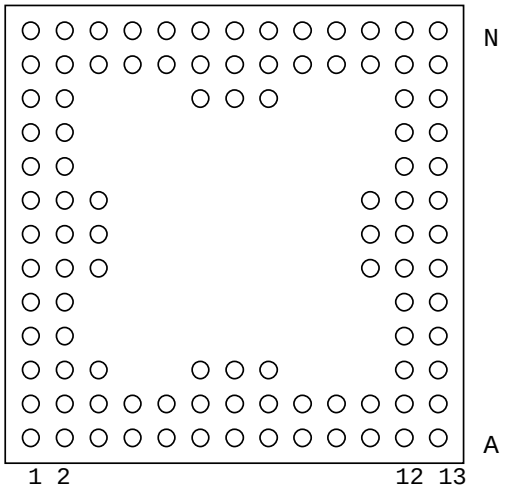

Figure 7 PGA100 package pin positions (bottom view)

TTCrx PIN ASSIGNMENTS (PRELIMINARY)

Pin assignments: sorted by pin number

Pin #	PGA100 Pos	Name	Type	Description
1	B2	Reset_b	in	General reset input
2	B1	PromD	in	Serial Prom data
3	C2	PromClk	out	Serial Prom clock
4	C1	PromReset	out	Serial Prom CE* and reset
5	D2	TTCReady	out	TTCrx is ready and stable
6	D1	D_VDD	pwr	Digital supply (I/O)
7	E2	D_GND	pwr	Digital ground (I/O)
8	E1	D_VDD	pwr_core	Digital supply (core)
9	F3	D_GND	pwr_core	Digital ground (core)
10	F2	A_GND	pwr	Analogue ground
11	F1	Res	in	Biasing input +
12	G2	Res_b	in	Biasing input -
13	G3	In	in	Input from PIN receiver +
14	G1	In_b	in	Input from PIN receiver -
15	H1	A_VDD	pwr	Analogue supply
16	H2	D_VDD	pwr	Digital supply (I/O)
17	H3	D_GND	pwr	Digital ground (I/O)
18	J1	D_VDD	pwr_core	
19	J2	D_GND	pwr_core	
20	K1	A_test0	in	Test pin 1
21	K2	A_test1	in	Test pin 2
22	L1	A_test2	out	Test pin 3
23	M1	A_test3	out	Test pin 4
24	L2	JTAGDO	out	JTAG
25	N1	JTAGDI	in	JTAG
26	M2	JTAGMS		JTAG
27	N2	JTAGCLK	in	JTAG
28	M3	Serial_B_Channel	out	Serial B channel
29	N3	BCnt<11>	out	Bunch counter / Ev Counter bus
30	M4	BCnt<10>	out	Bunch counter / Ev Counter bus
31	N4	D_VDD	pwr	Digital supply (I/O)
32	M5	D_GND	pwr	Digital ground (I/O)
33	N5	BCnt<9>	out	Bunch counter / Ev Counter bus
34	L6	BCnt<8>	out	Bunch counter / Ev Counter bus
35	M6	BCnt<7>	out	Bunch counter / Ev Counter bus
36	N6	BCnt<6>	out	Bunch counter / Ev Counter bus
37	M7	BCnt<5>	out	Bunch counter / Ev Counter bus
38	L7	BCnt<4>	out	Bunch counter / Ev Counter bus
39	N7	BCnt<3>	out	Bunch counter / Ev Counter bus
40	N8	BCnt<2>	out	Bunch counter / Ev Counter bus
41	M8	BCnt<1>	out	Bunch counter / Ev Counter bus
42	L8	BCnt<0>	out	Bunch counter / Ev Counter bus
43	N9	D_VDD	pwr	Digital supply (I/O)
44	M9	D_GND	pwr	Digital ground (I/O)
45	N10	BCntStr	out	Bunch counter strobe
46	M10	EvCntHStr	out	Event counter high strobe
47	N11	EvCntLStr	out	Event counter low strobe
48	N12	BCntRes	out	Bunch counter reset

49	M11	EvCntRes	out	Event counter reset strobe
50	N13	L1Accept	out	L1 accept strobe
51	M12	Brcst<7>	out	User defined broadcast bus
52	M13	Brcst<6>	out	User defined broadcast bus
53	L12	BrcstStr2	out	Strobe for user defined broadcast
54	L13	Brcst<5>	out	System broadcast bus
55	K12	Brcst<4>	out	System broadcast bus
56	K13	D_VDD	pwr_core	Digital supply (core)
57	J12	D_VDD	pwr	Digital supply (I/O)
58	J13	D_GND	pwr	Digital ground (I/O)
59	H11	D_VDD_C	pwr special	
60	H12	Clock40	out	40.08 MHz clock
61	H13	D_GND_C	pwr special	
62	G12	D_VDD_C	pwr special	Digital supply (I/O)
63	G11	Clock40Des1	out	Deskewed 40.08 MHz clock 1
64	G13	D_GND_C	pwr special	Digital ground (I/O)
65	F13	D_VDD_C	pwr special	Digital supply (I/O)
66	F12	Clock40Des2	out	Deskewed 40.08 MHz clock 2
67	F11	D_GND_C	pwr special	Digital ground (I/O)
68	E13	D_VDD	pwr	Digital supply (I/O)
69	E12	D_GND	pwr	Digital ground (I/O)
70	D13	D_GND	pwr_core	Digital ground (core)
71	D12	Brcst<3>	out	System broadcast bus
72	C13	Brcst<2>	out	System broadcast bus
73	B13	BrcstStr1	out	Strobe for system broadcast bus
74	C12	SinErrStr	out	Single bit error strobe
75	A13	DbErrStr	out	Double bit error strobe
76	B12	SubAddr<0>	out	External subaddress bus
77	A12	SubAddr<1>	out	External subaddress bus
78	B11	SubAddr<2>	out	External subaddress bus
79	A11	SubAddr<3>	out	External subaddress bus
80	B10	SubAddr<4>	out	External subaddress bus
81	A10	D_GND	pwr	Digital ground (I/O)
82	B9	D_VDD	pwr	Digital supply (I/O)
83	A9	SubAddr<5>	out	External subaddress bus
84	C8	SubAddr<6>	out	External subaddress bus
85	B8	SubAddr<7>	out	External subaddress bus
86	A8	DQ<0>	out	Data qualifier
87	B7	DQ<1>	out	Data qualifier
88	C7	DQ<2>	out	Data qualifier
89	A7	DQ<3>	out	Data qualifier
90	A6	DoutStr	out	Data strobe
91	B6	Dout<0>	out	Data output bus
92	C6	Dout<1>	out	Data output bus
93	A5	D_GND	pwr	Digital ground (I/O)
94	B5	D_VDD	pwr	Digital supply (I/O)
95	A4	Dout<2>	out	Data output bus
96	B4	Dout<3>	out	Data output bus
97	A3	Dout<4>	out	Data output bus
98	A2	Dout<5>	out	Data output bus
99	B3	Dout<6>	out	Data output bus
100	A1	Dout<7>	out	Data output bus

Pin assignments: sorted by position

Pin #	PGA100 Pos	Name	Type	Description
100	A1	Dout<7>	out	Data output bus
98	A2	Dout<5>	out	Data output bus
97	A3	Dout<4>	out	Data output bus
95	A4	Dout<2>	out	Data output bus
93	A5	D_GND	pwr	Digital ground (I/O)
90	A6	DoutStr	out	Data strobe
89	A7	DQ<3>	out	Data qualifier
86	A8	DQ<0>	out	Data qualifier
83	A9	SubAddr<5>	out	External subaddress bus
81	A10	D_GND	pwr	Digital ground (I/O)
79	A11	SubAddr<3>	out	External subaddress bus
77	A12	SubAddr<1>	out	External subaddress bus
75	A13	DbErrStr	out	Double bit error strobe
2	B1	PromD	in	Serial Prom data
1	B2	Reset_b	in	General reset input
99	B3	Dout<6>	out	Data output bus
96	B4	Dout<3>	out	Data output bus
94	B5	D_VDD	pwr	Digital supply (I/O)
91	B6	Dout<0>	out	Data output bus
87	B7	DQ<1>	out	Data qualifier
85	B8	SubAddr<7>	out	External subaddress bus
82	B9	D_VDD	pwr	Digital supply (I/O)
80	B10	SubAddr<4>	out	External subaddress bus
78	B11	SubAddr<2>	out	External subaddress bus
76	B12	SubAddr<0>	out	External subaddress bus
73	B13	BrcstStr1	out	Strobe for system broadcast bus
4	C1	PromReset	out	Serial Prom CE* and reset
3	C2	PromClk	out	Serial Prom clock
92	C6	Dout<1>	out	Data output bus
88	C7	DQ<2>	out	Data qualifier
84	C8	SubAddr<6>	out	External subaddress bus
74	C12	SinErrStr	out	Single bit error strobe
72	C13	Brcst<2>	out	System broadcast bus
6	D1	D_VDD	pwr	Digital supply (I/O)
5	D2	TTCReady	out	TTCrx is ready and stable
71	D12	Brcst<3>	out	System broadcast bus
70	D13	D_GND	pwr_core	Digital ground (core)
8	E1	D_VDD	pwr_core	Digital supply (core)
7	E2	D_GND	pwr	Digital ground (I/O)
69	E12	D_GND	pwr	Digital ground (I/O)
68	E13	D_VDD	pwr	Digital supply (I/O)
11	F1	Res	in	Biasing input +
10	F2	A_GND	pwr	Analogue ground
9	F3	D_GND	pwr_core	Digital ground (core)
67	F11	D_GND_C	pwr special	Digital ground (I/O)
66	F12	Clock40Des2	out	Deskewed 40.08 MHz clock 2
65	F13	D_VDD_C	pwr special	Digital supply (I/O)
14	G1	In_b	in	Input from PIN receiver -
12	G2	Res_b	in	Biasing input -
13	G3	In	in	Input from PIN receiver +
63	G11	Clock40Des1	out	Deskewed 40.08 MHz clock 1
62	G12	D_VDD_C	pwr special	Digital supply (I/O)

64	G13	D_GND_C	pwr special	Digital ground (I/O)
15	H1	A_VDD	pwr	Analogue supply
16	H2	D_VDD	pwr	Digital supply (I/O)
17	H3	D_GND	pwr	Digital ground (I/O)
59	H11	D_VDD_C	pwr special	
60	H12	Clock40	out	40.08 MHz clock
61	H13	D_GND_C	pwr special	
18	J1	D_VDD	pwr_core	
19	J2	D_GND	pwr_core	
57	J12	D_VDD	pwr	Digital supply (I/O)
58	J13	D_GND	pwr	Digital ground (I/O)
20	K1	A_test0	in	Test pin 1
21	K2	A_test1	in	Test pin 2
55	K12	Brcst<4>	out	System broadcast bus
56	K13	D_VDD	pwr_core	Digital supply (core)
22	L1	A_test2	out	Test pin 3
24	L2	JTAGDO	out	JTAG
34	L6	BCnt<8>	out	Bunch counter / Ev Counter bus
38	L7	BCnt<4>	out	Bunch counter / Ev Counter bus
42	L8	BCnt<0>	out	Bunch counter / Ev Counter bus
53	L12	BrcstStr2	out	Strobe for user defined broadcast
54	L13	Brcst<5>	out	System broadcast bus
23	M1	A_test3	out	Test pin 4
26	M2	JTAGMS		JTAG
28	M3	Serial_B_Channel	out	Serial B channel
30	M4	BCnt<10>	out	Bunch counter / Ev Counter bus
32	M5	D_GND	pwr	Digital ground (I/O)
35	M6	BCnt<7>	out	Bunch counter / Ev Counter bus
37	M7	BCnt<5>	out	Bunch counter / Ev Counter bus
41	M8	BCnt<1>	out	Bunch counter / Ev Counter bus
44	M9	D_GND	pwr	Digital ground (I/O)
46	M10	EvCntHStr	out	Event counter high strobe
49	M11	EvCntRes	out	Event counter reset strobe
51	M12	Brcst<7>	out	User defined broadcast bus
52	M13	Brcst<6>	out	User defined broadcast bus
25	N1	JTAGDI	in	JTAG
27	N2	JTAGCLK	in	JTAG
29	N3	BCnt<11>	out	Bunch counter / Ev Counter bus
31	N4	D_VDD	pwr	Digital supply (I/O)
33	N5	BCnt<9>	out	Bunch counter / Ev Counter bus
36	N6	BCnt<6>	out	Bunch counter / Ev Counter bus
39	N7	BCnt<3>	out	Bunch counter / Ev Counter bus
40	N8	BCnt<2>	out	Bunch counter / Ev Counter bus
43	N9	D_VDD	pwr	Digital supply (I/O)
45	N10	BCntStr	out	Bunch counter strobe
47	N11	EvCntLStr	out	Event counter low strobe
48	N12	BCntRes	out	Bunch counter reset
50	N13	L1Accept	out	L1 accept strobe

Appendix

TTCrx Test Board

To facilitate testing of the current TTCrx version a PCB test board was designed and manufactured. It is available to designers wishing to integrate the TTCrx IC in their systems. The TTCrx test board is described in this appendix.

TEST BOARD

The TTCrx test board schematic is shown in Figure 8 and the placement of components in the board is represented in Figure 9 and Figure 10. The test board contains the TTCrx IC, an integrated detector/preamplifier (Honeywell), a serial configuration PROM (XC1736D), a fibre optic post-amplifier (NE5225D) and an ECL to TTL converter (10H125). This arrangement allows the TTCrx to be used with

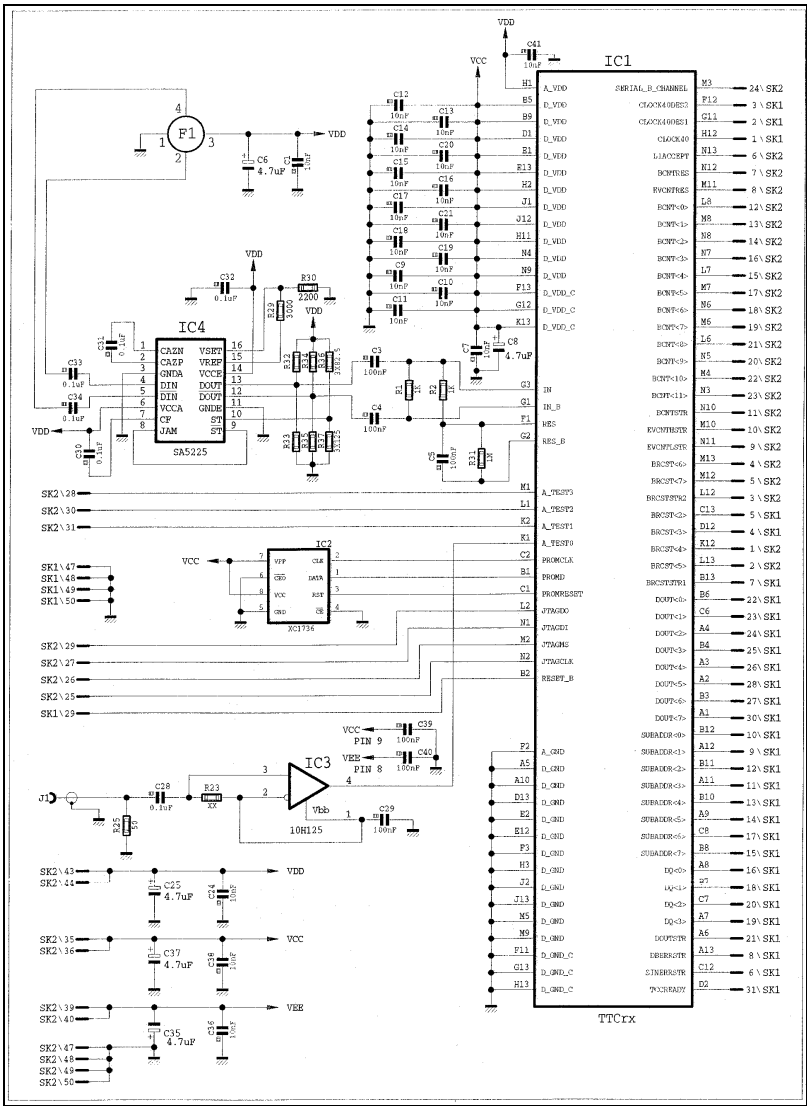

Figure 8 TTCrx test board schematic

either an optical signal, using the optical preamplifier, or with an electrical signal, using the pseudo ECL electrical input. The electrical input is terminated with a 50Ω resistor to ground and the signal is AC coupled to the ECL/TTL converter input. To enable operation using the this input, bit number 23 (“ref_gen_mux”) in the serial configuration PROM has to be set to “1”[13].

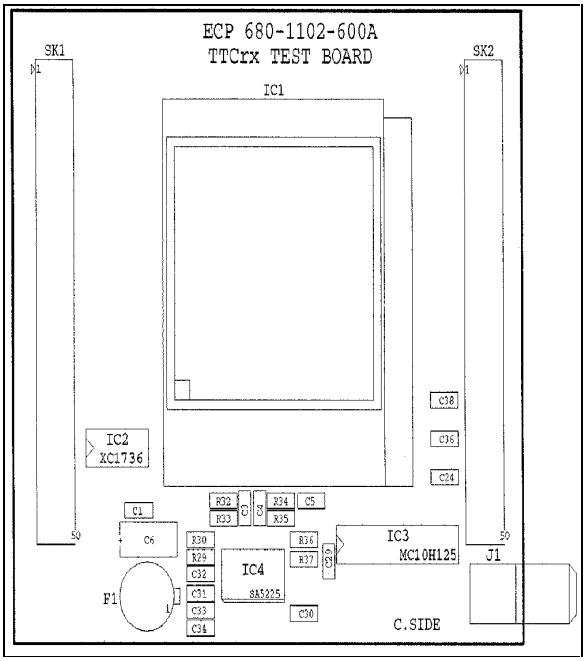

Figure 9 Components placement (c_side)

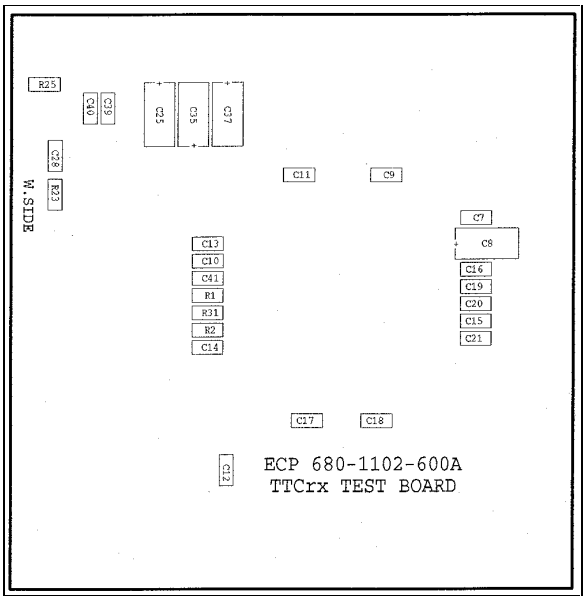

Figure 10 Components placement (w_side)

[13] For more information on the serial configuration PROM programming see “ Configuration register”

Test board pin assignments

Connector 1

Pin #	**Name**	**Description**
1	Clock40	40.08MHz clock
2	Clock40Des1	Deskewed 40.08MHz clock 1
3	Clock40Des2	Deskewed 40.08MHz clock 2
4	Brcst<3>	Broadcast bus
5	Brcst<2>	Broadcast bus
6	SinErrStr	Single error strobe
7	BrcstStr1	System broadcast strobe
8	DbErrStr	Double error strobe
9	SubAddr<1>	Subaddress bus
10	SubAddr<0>	Subaddress bus
11	SubAddr<3>	Subaddress bus
12	SubAddr<2>	Subaddress bus
13	SubAddr<4>	Subaddress bus
14	SubAddr<5>	Subaddress bus
15	SubAddr<7>	Subaddress bus
16	DQ<0>	Data qualifier bus
17	SubAddr<6>	Subaddress bus
18	DQ<1>	Data qualifier bus
19	DQ<3>	Data qualifier bus
20	DQ<2>	Data qualifier bus
21	DoutStr	Data strobe
22	Dout<0>	Data bus
23	Dout<1>	Data bus
24	Dout<2>	Data bus
25	Dout<3>	Data bus
26	Dout<4>	Data bus
27	Dout<6>	Data bus
28	Dout<5>	Data bus
29	Reset_b	General reset input
30	Dout<7>	Data bus
31	TTCReady	TTCrx ready
47	GND	Ground

48	GND	Ground
49	GND	Ground
50	GND	Ground

Connector 2

Pin #	**Name**	**Description**
1	Brcst<4>	Broadcast bus
2	Brcst<5>	Broadcast bus
3	BrcstStr2	User broadcast strobe
4	Brcst<6>	Broadcast bus
5	Brcst<7>	Broadcast bus
6	L1Accept	L1 accept strobe
7	BCntRes	Bunch counter reset
8	EvCntRes	Event counter reset
9	EvCntLStr	Event counter low strobe
10	EvCntHStr	Event counter high strobe
11	BCntStr	Bunch counter strobe
12	BCnt<0>	Bunch counter bus
13	BCnt<1>	Bunch counter bus
14	BCnt<2>	Bunch counter bus
15	BCnt<4>	Bunch counter bus
16	BCnt<3>	Bunch counter bus
17	BCnt<5>	Bunch counter bus
18	BCnt<6>	Bunch counter bus
19	BCnt<7>	Bunch counter bus
20	BCnt<9>	Bunch counter bus
21	BCnt<8>	Bunch counter bus
22	BCnt<10>	Bunch counter bus
23	BCnt<11>	Bunch counter bus
24	Serial_B_Channel	Serial B channel
25	JTAGCLK	Not used
26	JTAGMS	Not used
27	JTAGDI	Not used
28	A_test3	Test pin 3
29	JTAGD0	Not used
30	A_test2	Test pin 2

31	A_test1	Test pin 1
35	A_VDD	Analogue supply
36	A_VDD	Analogue supply
39	VEE	ECL supply
40	VEE	ECL supply
43	D_VDD	Digital supply
44	D_VDD	Digital supply
47	GND	Ground
48	GND	Ground
49	GND	Ground
50	GND	Ground

References

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